German Research Center for Artificial Intelligence

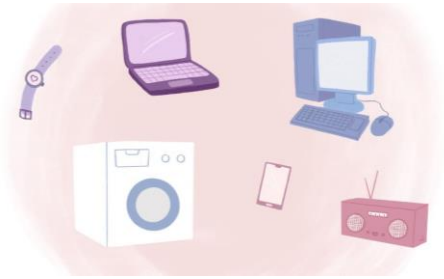
Cyber-Physical Systems

Verification and Virtual Prototyping for RISC-V Systems

The Problem

Embedded and cyber-physical systems have become small, versatile and powerful. They are used in a wide range of application areas, from smart homes to communication, transportation and manufacturing.

This versatility requires an adaptable and flexible architecture, as different application areas bring different requirements.



Unfortunately, the architecture of processors available on the market is dominated by a few manufacturers. Their systems are proprietary, closed, and protected by patents. This makes it difficult to develop new processors and systems-on-chip for new applications, and thus represents an obstacle to innovation. How can we surmount this hurdle?

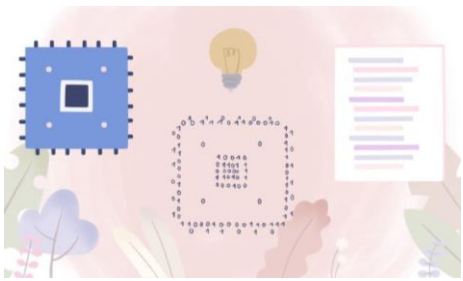
RISC-V and its Advantages

Inspired by the success of open source software (such as the Linux operating system, which forms the core of the Android operating system), open designs for hardware have recently emerged. Among these, the RISC-V architecture, has gained tremendous momentum over the last years.

RISC-V has been under development at the University of California at Berkeley since 2010. It is an instruction set architecture: it defines the instructions the microprocessor can be programmed with, including their binary format, and how the microprocessor presents itself to the software (which registers it has and how they are to be used, for example).

For this architecture, different manufacturers can provide hardware implementations (processors) on the one hand, and software manufacturers can develop programs that run on them on the other. The open, standardized and patent-free architecture thus allows a broad, rich ecosystem of hardware and software.

The main advantages of the RISC-V architecture are thus: it is scalable and can be adapted to the respective requirements with different word widths; it is modular and easily expandable; and it is future-proof because it is standardized, vendor-independent and open.



Our Contributions

The Cyber-Physical Systems research department of the German Research Center for Artificial Intelligence is contributing to the success of RISC-V in several projects, and will present this work at Hannover Messe 2021.
In the HEP project, a formally verified RISC-V processor including a crypto accelerator is being developed together with academic and application partners from the automotive industry, together with an open source tool chain. Moreover, in the VerSys project, a SystemC-based virtual prototype for RISC-V systems is being further developed into an industrial-grade verification platform that is consistent, correct, and as scalable and modular as the RISC-V architecture, and can be easily adapted by users to their requirements.

Contact

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