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RESEARCH ARTICLE

Adaptation of a Real-Time Deep Learning Approach With an Analog Fault Detection Technique for Reliability Forecasting of Capacitor Banks Used in Mobile Vehicles

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ABSTRACT The DC-Link capacitor is defined as the essential electronics element which sources or sinks the respective currents. The reliability of DC-link capacitor-banks (CBs) encounters many challenges due to their usage in electric vehicles. Heavy shocks may damage the internal capacitors without shutting down the CB. The fundamental development obstacles of CBs are: lack of considering capacitor degradation in reliability assessment, the impact of unforeseen sudden internal capacitor faults in forecasting CB lifetime, and the faults consequence on CB degradation. The sudden faults change the CB capacitance, which leads to reliability change. To more accurately estimate the reliability, the type of the fault needs to be detected for predicting the correct post-fault capacitance. To address these practical problems, a new CB model and reliability assessment formula covering all fault types are first presented, then, a new analog fault-detection method is presented, and a combination of online-learning long short-term memory (LSTM) and fault-detection method is subsequently performed, which adapt the sudden internal CB faults with the LSTM to correctly predict the CB degradation. To confirm the correct LSTM operation, four capacitors degradation is practically recorded for 2000-hours, and the off-line faultless degradation values predicted by the LSTM are compared with the actual data. The experimental findings validate the applicability of the proposed method. The codes and data are provided.

INDEX TERMS Capacitor-bank, deep learning, power system reliability, artificial intelligence (AI), machine learning, electronics.

NOMENCLATURE

CB	Capacitor bank.
C	Capacitance of each internal capacitor (F).
C_{CB}	Capacitance of CB (F).
i	Total series capacitors in a column of the CB matrix.
j	Total number of columns of the CB matrix.
n	Column number in the CB matrix.
m	Row number in the CB matrix.

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C_{nm}	Capacitor in column n and row m.
x	Number of capacitors that are shorted.
x_n	Number of capacitors that are shorted in column n.
y	Number of capacitors that are opened.
y_n	Number of open-circuit faults in each column of n.
ESR_{CB}	Equivalent series resistance of the CB (Ω).
$I_{peak,CB}$	Capacitor bank peak output current (A).
V_O	Maximum capacitor rated voltage (V).
L	Lifetime (h).
B	Rated lifetime (h).
E_a	Activation energy (1.4 eV).
k	Boltzmann's constant (8.617E-5 eV/K)
T_A	Application temperature (Celsius).
T_C	Category temperature (Celsius).
V_R	Rated voltage of capacitor (V).
ESR_{DC}	DC Equivalent series resistance (Ω).
Δt	Time deviation (s)
ESR_t	ESR value at the time t (Ω).
ESR_0	Initial ESR (Ω).
E	Activation energy/Boltzmann constant (4700).
x_t	Input vector to the LSTM.
t	Time (h).
V_{Cnm}	Voltage of capacitor in column n and row m (V).
V_{CB}	Capacitor bank voltage (V).
ΔV	Deviation of voltage (V).
λp	Failure rate (Failures/(10^6Hours)).
λ_b	Base failure rate (Failures/(10^6Hours)).
π_{CV}	Capacitance factor of a capacitor.
π_Q	Quality factor.
π_E	Environment factor.
T	Ambient temperature (Celsius).
S	Stress voltage.
$R(t)$	Reliability in time t (%).
MTTF	Mean Time to Failure (h).
δ	Impedance phase angle.
V	Operating voltage of electrolyte capacitor (V).
C_t	LSTM cell state vector.
h_t	LSTM hidden state vector.
h_{t-1}	LSTM output function at earlier time.
C_{t-1}	LSTM cell state vector at earlier time.
MAPE	Mean absolute percentage error (%).
MSE	Mean squared normalized error.
RMSE	Root mean squared normalized error.
ME	Maximum error.
i_C	Capacitor current (A).
C_d	Ideal capacitance
f	Frequency (Hz).
X_{Cd}	Impedance of capacitor (Ω).
A_t	Actual value.
F_t	Forecast value.
n	Number of fitted points.

I. INTRODUCTION

The utilization of capacitor banks (CBs) as energy storage in power grids, railroad systems, and electric vehicles (EVs) has been increased significantly over the past few years [1]. Over the recent decades, CBs have become important due to applications in DC link inverters, microgrids, switched capacitors, and Metro system drives, and various sections of EVs [2]; thus, through the sensitivity of these applications, their diagnosis is also very important. As far as CBs are capable of storing energy, their fast energy compensation plays an essential role in controlling the frequency of microgrids, especially when it develops into renewable energy sources [3]. So far, different models have been proposed for simulating different CB situations. In [4] and [5], different models and technologies of power semiconductors and CBs have been introduced, which can be used in power grids for renewable energy generation. The CB is typically a combination of series-parallel electrolytic capacitors [1]. The electrolytic capacitor performance is complicated and is strongly influenced by operating conditions such as frequency, current, voltage, and ambient temperature. Furthermore, their degradation process affects the electrolytic capacitors, reducing reliability, lifetime, and output. Simple equivalent circuit of a capacitor is shown in Figure 1(a). Cd and Equivalent series resistance (ESR) are the main factors responsible for the degradation of the CB, where the ESR is the limiting factor of the output current of the CB. Much research has focused on the study of electrolyte capacitor degradation [1], [6], [7], [8], [9], [10], [11]. For instance, Authors in [6] improve the CB aging model considering the temperature, variable load, and constant charge. Also, this work explores the CB aging behavior by periodically monitoring the electrical and electrochemical health status. In addition, numerous research studies use artificial intelligence (AI) to predict degradation and lifetime of the CBs [7]. With the correct prediction of ESR and capacitance degradation, the reliability, lifetime and peak output current of the CB can be calculated. In [8] and [9] off-line learning data were used to predict the degradation independent of sudden failures. However, a sudden fault may occur in the internal capacitors of the CB. The short/open-circuit faults might occur for several reasons: current surges, electrolytic capacitor swelling, and material oxidation used in the electrolytic capacitor [1]. Other unforeseen faults can sometimes befall (e.g., a heavy shock to the CBs), which might damage the internal structure of the CBs. When a fault occurs, the reliability, degradation value, and storage energy of the CB will change, so the off-line AI training may not be used and the learning data must be updated after the fault.

While many models for capacitors have been presented to evaluate reliability and degradation [10], [11], it is necessary to develop a model of the CB that includes all types of short-circuit and open-circuit faults of the internal capacitors to predict degradation correctly. Using an appropriate CB model and adapting a fast fault detection method with a suitable AI method, the degradation may be predicted, which will evaluate the CB's reliability, peak current, and maximum stored energy.

This manuscript is a sequel to the 13-level inverter [12], which aims to apply long short-term memory (LSTM) to

TABLE 1. The advantages and disadvantages of the LSTM.

Advantages	1) Ability to learn the feature of sequential time series data due to their structural compositions. 2) Enhancing the disappearing gradient issue of traditional RNN. 3) Ability to learn both long-term and short-term dependencies. 4) Insensitivity to the length of the gap.
Disadvantages	1) High memory requirements, high computational complexity. 2) Need for a long time to train the models.

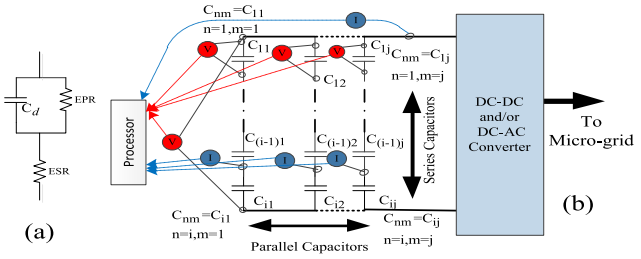

FIGURE 1. (a) Equivalent model of a capacitor, and (b) CB structure.

sudden faults. Hochreiter and Schmidhuber first proposed the deep learning method in 1997 [13]. The LSTM in deep learning is a subset of artificial recurrent neural networks (RNN). In contrast to feedforward neural networks, LSTM possesses feedback in its structure. This neural network is appropriate for sequential data and is among the most suitable networks based on time series data [14]. The decreasing gradient problem in the RNN is also solved in this network [15]. Table 1 shows the advantages and disadvantages of the LSTM [16], [17], [18], [19]. High memory requirements, high computational complexity, and a large number of data are the main disadvantages of the LSTM. The method presented in this paper covers major disadvantages of the LSTM, meaning that both the complexity and need for numerous data are reduced and eliminated respectively.

A. MOTIVATION AND INCITEMENT OF SUDDEN FAULTS

In [16], [17], [18], [19], and [20], several deep learning methods have been discussed for predicting the corresponding parameters such as remaining useful life and health status of batteries, which are similar to CB degradation. These methods include the LSTM, bi-directional-LSTM, adaptive boosting (AB), support vector regression (SVR), convolutional neural network (CNN), multi-layer perceptron (MLP), Elman recurrent neural network (ERNN), echo state network (ESN), gated recurrent unit network (GRU), temporal convolutional network (TCN), back-propagation neural networks (BPNN), k-nearest neighbor (KNN), and input selection hybrid forecasting (IS-HF). Among all of them, the LSTM method have been exhibited the best results. In view of these results and the advantages listed in Table 1, we selected the LSTM for this study.

Most of the predictions made by the LSTM in studies [16], [17], [18], [19] are based on past data, and sudden failures are disregarded. It seems that the impact of sudden faults on the CB is a gap that has not been fully answered. The collision's effects on the ground resulted in a change in the capacitor bank's capacitance and ESR, although the CB's appearance was unchanged. Two main reasons exist for using equivalent capacitance and equivalent ESR, which are applied in fault diagnosis and higher accuracy reliability evaluation [26]. Note that applying Equivalent Capacitance and ESR allows for a more accurate capacitor bank reliability and lifetime calculation. Also, it facilitates faster fault detection and prevention of capacitor bank explosion. In [27], a new analysis based on an offline look-up table was proposed to predict the lifetime performance of multiple CB designs. A novel methodology for internal failure detection in large shunt CBs has been introduced in [28], where the lookup table is adopted for scaling data. However, the look-up-table-based methodologies are not effective because of the changes in the CB's voltages and various levels of degradation of the capacitors under different environmental conditions. To address the above problems, numerous research studies focused on artificial intelligence (AI) to predict the degradation and lifetime of the CBs according to the change in the environment condition.

The reliability of the capacitor depends on the capacitance, and by predicting the capacitance, the reliability and lifetime are possible to be predicted. When a sudden fault occurs, the capacitance of the CB changes, and thus the capacitance prediction before the fault occurred becomes invalid, which means that the reliability and lifetime of the CB become invalid. The reason is that the prediction was based on the pre-fault data and the post-fault data is different from the pre-fault data, so the Deep Learning LSTM needs to be re-trained with the new post-fault data to provide a correct prediction of the capacitance. The training data required for the LSTM is determined by the detection of the fault type, i.e., by detecting the fault type, the new capacitance value of the capacitor bank is supplied to the LSTM as new training data. The pre-fault data will cause errors in the prediction. Therefore, the pre-fault data should be cleared, and by knowing the type of the fault, the correct capacitance value will be given to the LSTM as new training data, and as a result, the new capacitance value will be predicted.

In our paper, the hypothesis is based on the CB's sudden unforeseen failure, whereas the trained data is updated immediately, and the past data is excluded based on the proper operation of the CB; thus, the prediction will be based on the actual conditions.

Considering an EV using a CB as storage energy, suddenly it crashes with another car and the CB damages harshly. This kind of accident is not predictable, but the impulse that indirectly enters the CB can cause an internal fault. Our work investigates these kinds of sudden unforeseen faults and faults on the CB's internal capacitors. Also, forecasting the peak output current and the reliability of CB following the fault is carried out using LSTM in real-time.

B. LITERATURE REVIEW OF THE ONLINE LSTM

Based on the LSTM and employed time-series data, [21] predicted the operation of wind turbines and detected the

fault based on the difference between actual data and the predicted data. Based on raw data and dynamic new matching data, this study presents a fault diagnosis method with the LSTM. The proposed method has been implemented in the Tennessee Eastman benchmark. The data are verified in both online and offline modes. The main difference of [22] from presented work is the use of the LSTM in a different structure. proposed method is tested practically in a subsystem, and practice tests are also conducted to make an accurate forecast and evaluation. Some of the faults mentioned in our study do not shut down the system but weaken the CB's performance. The following difference is related to the type of fault detection. In presented work, analog fault detection using an electronic circuit combines with the LSTM prediction; Thus, the detection speed significantly increases (less than 1 *ms*), but in [22], fault detection is accomplished only with the help of the LSTM. Reference [23] presents a method for detecting high current DC faults using the combined RNN based auto encoder (AE) and the LSTM. Evaluation of the suggested method using pulse load and proving the performance correctness in distinguishing the pulse current from the short-circuit fault current is also part of the tasks performed in this paper. The load current is monitored and recorded to detect faults. This paper's central mission of deep learning is fault detection, while time series prediction is not implemented. Among the advantages of presented study compared to [23], the following can be asserted: i) despite fault detection, lifetime and capacitance of CB prediction are also implemented, ii) the proposed method can detect both fault and fault type. In [24], the authors investigated the diagnosis of open circuit faults of switches used in DFIG wind turbine back-to-back converters using the LSTM. Semiconductor switches are more likely to be short-circuited after a fault compared with open-circuit. Therefore, it might be more proper to consider short-circuit faults plus monitoring and diagnosing switch open-circuit faults.

C. CONTRIBUTION AND PAPER ORGANIZATION

In reviewing the literature on LSTM and CB fault detection, the following gaps were identified. 1) Quantitative research has been conducted in the field of fault detection, which includes the combination of analog fault detection and artificial intelligence. By combining these two methods, the shortcomings of each method can be compensated by the other, and the speed and accuracy can be increased. 2) The lack of a capacitor bank model that includes all types of internal capacitor faults. 3) The effects of sudden faults on LSTM forecasting have been poorly researched. In the case of a sudden fault, the predicted value differs greatly from the actual value and the learning data must be updated. Little research has been done on how to update the training data in online-LSTM.

The main novelties of this paper are i) introducing a new real-time fault detection technique to detect both the fault and type of the fault, ii) combining LSTM technique with novel analog control to online-forecasting the capacitance and equivalent series resistance (ESR) due to sudden faults, and iii) proposing a new CB model including short-circuit and open-circuit faults.

This paper consists of the following sections: I) investigating the effects of open circuit and short circuit fault of internal capacitors on the reliability and peak output current of the CB, II) CB modeling in short circuit fault and open circuit fault of series-parallel combined capacitors, III) introduction a new method for detecting the type and location of a faulty-internal-capacitor in the CB, IV) effect of ESR and capacitance degradation on reliability and peak current of a CB considering fault, V) application of the real-time LSTM deep learning method in predicting ESR and capacitance degradation considering all types of sudden faults, VI) experimental test on a small scale to evaluate ESR and capacitance degradation and validate the LSTM method, VII) experimental test to validate the proposed method to detect the type and location of faulty-capacitors of the CB, and IX) discussion on experimental test results and peak current calculations of the CB and its reliability after some random faults. Finally, the result of this article might be generalized to the battery as well. Currently, batteries are being used more than CBs in EVs.

II. EFFECTS OF OPEN-CIRCUIT AND SHORT-CIRCUIT FAULTS

There are two types of short-circuiting and open-circuit faults in the CB system, and each has different adverse effects on the system. The capacitor's equivalent circuit and the structure of a CB composed of electrolytic capacitors are shown in Figure 1. The series capacitors (n) range from 1 to i, and each column (m) from 1 to j.

Due to the distinct impacts of various faults on the CBs, the CB model seems necessary to achieve reliability and peak current calculations; thus, a novel model is proposed by considering the effect of faults.

A. NEW MODELING OF CAPACITOR BANK

1) EQIVALENT CAPACITANCE

According to Figure 1(b), if the internal capacitors of the CB are assumed to be matrix elements while the improved modeling of the CB including capacitance and ESR are performed. Here it is assumed that all internal column capacitors are equal; Thus, the capacitance of the fault-free CB is equivalent to:

$$C_{\mathrm{CB}} = j \times \frac{C}{i} \tag{1}$$

The capacitance of the CB will be equal to:

$$C_{\mathrm{CB}} = \sum_{n=1}^{j-y} \frac{C_{\mathrm{nm}}}{i}, \mathrm{m} = 1. \tag{2}$$

Equation (2) is for calculating the CB capacitance in the absence of short-circuit fault. More precisely, the equation will be, as in (3), shown at the bottom of the next page.

Therefore, the capacitance fault impact factor is obtained by dividing the capacitance gained after the fault via the fault-free capacitance value:

$$\mathrm{FIF}_C = \frac{\sum_{n=1}^{j} \frac{y_n \times C_{\mathrm{nm}}}{i - x_n}}{j \times \frac{C}{i}}. \tag{4}$$

2) EQIVALENT ESR

Figure 1(a) shows the equivalent circuit of the capacitor. After a short-circuit fault, the C_d is cleared, and only the ESR remains in the circuit. In case of no-fault, the equivalent ESR of a CB is:

$$\mathrm{ESR}_{\mathrm{CB}} = i \times \left(\mathrm{ESR}/_{j}\right), \tag{5}$$

If an open circuit fault occurs, the capacitors of the related column will be disconnected, and the ESR is equal to, as in (6), shown at the bottom of the next page.

The ESR fault impact factor is gained by dividing the ESR obtained after the fault has occurred by the ESR value without fault. Therefore, the maximum output current of the CB, after the x_n number of short circuit faults in the nth column, and the y_n capacitor open circuit fault in the nth column, will be as follows:

$$I_{\mathrm{peak,CB}} = \frac{1}{2}\left(\frac{\sum_{n=1}^{j} \frac{y_n \times C_{\mathrm{nm}}}{i - x_n} \times V_R}{\Delta t + \left(\left(\sum_{n=1}^{i} \frac{y_n \times \mathrm{ESR}_{\mathrm{nm}}}{j}\right) \times \left(\sum_{n=1}^{j} \frac{y_n \times C_{\mathrm{nm}}}{i - x_n}\right)\right)}\right), \tag{7}$$

B. THE EFFECT OF FAILURES OF AN INTERNAL CAPACITOR IN CB

1) IDENTIFICATION OF FAULT TYPE AND LOCATION

Three significant reasons can be provided for the reasons why fault detection is essential. First, the fault leads to a change in CB lifetime and output current. Second, Troubleshooting and accurate prediction of a lifetime and maximum current can keep the system stable. Third, CB system recovery is faster, and more significant system faults are avoided. Figure 1(b) shows the monitoring approach of the current and voltage of the CB, the current flowing through each series of capacitors, and the voltage of the first capacitor of each column. One of the benefits of the proposed method is that it is possible to use inexpensive voltage and current sensors commercially available for fault detection. The total voltage sensing of the CB module is carried out, and also, in each column of series-capacitors, only the voltage of the first capacitor is measured. With this voltage sampling, the effects of fault can be identified. The proposed fault detection method and flowchart are prepared based on these tips. Depending on the voltage change that occurs on each capacitor of the voltage sampler, it is possible to determine the column in the fault that has occurred.

2) FAULT DETECTION FLOWCHART

If the CB is considered a matrix, m is a row, and n is a column. The capacitor voltage is not always regular and might fluctuate depending on the application. To make experimental tests, fluctuating CB voltage was selected, which is the most challenging condition of the test. Since there is a delay in measuring the sampling voltage, and the voltage also fluctuates, the ΔV range is taken into account. Therefore, instead of a number, there is a comparable voltage range. The magnitude of this ΔV depends on the type of CB application in the electronic system.

a: CALCULATION OF THE ΔV RANGE

The minimum value of the sampled capacitor voltage (V_{Cmn}) is the voltage of the capacitor bank with no fault occurrence. Any short circuit in a column capacitor of the capacitor bank will cause the CB voltage to be distributed to the rest of the series capacitors, increasing the remaining voltage of the capacitors. Therefore, the value of ΔV should be as low as possible so that there is no interference between the voltage measurement ranges in each block and so that the fault detection process can be performed correctly. Equations (8) and (9) show the voltage range of the capacitor V_{Cmn} in the normal state without a fault and in the state of a short-circuit fault.

$$\frac{V_{\mathrm{CB}}}{i} - \Delta V < V_{\mathrm{Cmn}} < \frac{V_{\mathrm{CB}}}{i} + \Delta V (\text{No SC fault}), \tag{8}$$

$$\frac{V_{\mathrm{CB}}}{i-1} - \Delta V < V_{\mathrm{Cmn}} < \frac{V_{\mathrm{CB}}}{i-1} + \Delta V (\text{One SC fault}). \tag{9}$$

If (10) holds, there is no interference between the ranges:

$$\frac{V_{\mathrm{CB}}}{i-1} + \Delta V < \frac{V_{\mathrm{CB}}}{i} - \Delta V. \tag{10}$$

Simplification yields the following relationship:

$$|\Delta V| < \frac{V_{\mathrm{CB}}}{2i\,(i-1)}, \tag{11}$$

where i is the total number of series capacitors in a capacitor bank column. Therefore, the value of ΔV depends on the voltage of the capacitor bank and the number of capacitors connected in series, and if the voltage is constant, the value of ΔV can be considered constant. If the voltage of the capacitor bank is variable, the lowest value of the voltage of the capacitor bank should be considered in relation (11).

$$C_{\mathrm{CB}} = \left[\sum_{n=1}^{j} \frac{y_n \times C_{\mathrm{nm}}}{i - x_n}, \begin{cases} m = 1 \\ y_n = 0, \text{For open circuit fault of capacitor in column n} \\ y_n = 1, \text{For non-faults of open circuit in column n} \end{cases}\right]. \tag{3}$$

In the experimental setup of our article, i=3 and VCB=24 V, thus according to (11):

$$|\Delta V| < \frac{24}{2 \times 3 \times (3-1)} \Rightarrow |\Delta V| < 2(\mathrm{V}) \tag{12}$$

It is preferable to set the value of ΔV slightly smaller than the limit value so that the fault detection process can be performed correctly. In this study the ΔV=1.

3) FAULT DETECTION PROCESS

Figure 3(b) shows the flowchart of the online fault detection. First, the CB voltage and the voltages of the first capacitor of each column are measured.

***Block 1*:** First, a voltage comparison is performed to detect a short-circuit fault in column *j*. The value of *n* increases from column 1 to column *j*; therefore, the total voltage comparison of the first capacitor with the specified range is performed. A matrix will be formed by comparing the voltage arrays of the first row to the voltage range. This voltage range is the voltage obtained by dividing the voltage of the CB by the number of capacitors in the series. If there is no short-circuit fault, all capacitors work in a specific voltage range. In this case, If the current in the column is non-zero, it implies that no short circuit fault exists and the measurement process repeats.

Block 2: If voltage is not within the allowed range; thus, the voltage comparison takes place in block 2. If the voltage is $V_{\mathrm{Cmn}} \geq \left(V_{\mathrm{CB}}/i\right) + \Delta V$, two situations might occur:

1) shorting one capacitor of column *n* series, 2) opening one capacitor of column *n*. If the output current of this column is zero, this means that a capacitor open circuit fault has occurred, and if there is a current, at least one capacitor in this column is short-circuited.

Block 3: If the condition of block 3 is satisfying, a capacitor of the nth column of the connection is shorted, and if this condition is not satisfactory, the state of block four should be checked.

Block 4: Block four monitors how many capacitors in the nth column are shorted. If none of the provided conditions occur, it means that the CB is disconnected or permanently interrupted. MIL-STD-11991 recommends that the applied voltage of the capacitor should be half the rated voltage of the capacitor [25]. Thus, if half of the capacitors in a column are shorted, the CB should stop working immediately; otherwise, the CB will explode or burst.

III. EFFECT OF ESR AND CAPACITANCE DEGRADATION CONSIDERING FAULTS

The reliability of the CB decreases over time. Based on the MIL-HDBK-217 standard, the reliability of the capacitor depends on the temperature, the voltage stress on the capacitor, the environment, and the quality of the capacitor [26]. Many component datasheets state the lifetime of capacitors. However, Standard 217 can also calculate electronic components' failure probability, reliability, and lifetime [26]. The standard MIL-HDBK-217 seems sufficient to investigate the effects of time-lapse on ESR and capacity degradation. Note that standard 217 is only enough if only one CB is considered. Equation (13) is used to determine the failure rate of aluminum, dry electrolyte, and polarized capacitors:

$$\lambda_p = \lambda_b \pi_{\mathrm{CV}} \pi_Q \pi_E. \tag{13}$$

The π_{CV} and λ_b are calculated by this equation:

$$\pi_{\mathrm{CV}} = 0.32C^{0.19}, \tag{14}$$

$$\lambda_b = 0.0028\left[\left(\frac{S}{0.55}\right)^3 + 1\right] \times \exp\left(4.09\left(\frac{T+273}{358}\right)^{5.9}\right). \tag{15}$$

S is calculated by:

$$S = \frac{V_{\mathrm{applied}}}{V_{\mathrm{nominal}}}. \tag{16}$$

Based on [26], for non-military capacitors $\pi_Q = 10$, and $\pi_{\mathrm{E}} = 1$ in ground-based systems. The reliability and lifetime relationships are obtained according to the following equations [26]:

$$R(t) = e^{-\lambda t}, \tag{17}$$

$$\mathrm{MTTF} = \frac{1}{\lambda}. \tag{18}$$

Equation (14) shows the dependence of the reliability on the capacitance of the capacitor and (16) also shows the dependence of the reliability on voltage stress.

Under the same operating voltage, the greater the number of series capacitors, the greater the reliability. In a 24-volt CB, there might be two connected in each column and three capacitors in series. Figure 2 shows comparison curves of CBs with 4 × 3 capacitors and 4 × 2 capacitors. Clearly, by increasing the number of capacitors connected in series, the reliability increases; The reason is to decrease the voltage stress on each capacitor. The lower the voltage stress, the better the reliability. Table 2 illustrates the reliability of each capacitor in 4 × 3 and 4 × 2 arrangements of the capacitor bank.

There is both the possibility of a short-circuit fault of the internal capacitors and the possibility of an open-circuit fault in the capacitor bank. Therefore, from the digital viewpoint,

$$\mathrm{ESR_{CB}} = \left[\sum_{n=1}^{i} \frac{y_n \times \mathrm{ESR_{nm}}}{j}, \quad \begin{cases} m = 1 \\ y_n = 0, \text{For open circuit fault in column n} \\ y_n = 1, \text{For non-faults of open circuit in column n} \end{cases}\right]. \tag{6}$$

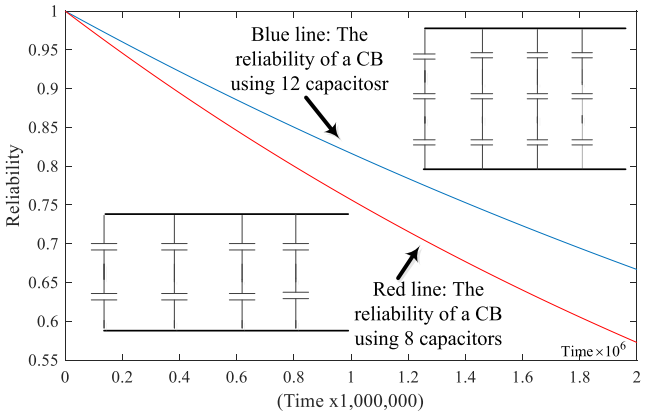

FIGURE 2. Comparison of the reliability of capacitor banks including capacitors using 4 × 3 and 4 × 2 layout.

TABLE 2. The values of the reliability assessment parameters of one capacitor taken from MIL-HDBK-217.

CB array	Temp. (°C)	S based on (16)	λ_b	π_{CV}	π_Q	π_E	λ_p	Reliability of one capacitor
4×2 array	25	0.24	0.0121	0.0861	10	1	0.0104	$R(t)=e^{-0.0104t}$
4×3 array	25	0.16	0.0115	0.0861	10	1	0.0091	$R(t)=e^{-0.0091t}$

either a short-circuit fault or an open-circuit fault occurs in each internal capacitor. When an open circuit occurs, the internal capacitor disconnects from the other capacitors, so that the entire column in CB is disconnected. Assuming that the identical internal capacitors may fall into open circuit faults, the following reliability relationship is obtained for a CB:

$$R_{\mathrm{CB,OC}} = 1 - \prod_{n=1}^{j}\left(1 - \prod_{m=1}^{i}\left(1 - R_{\mathrm{mn}}(t)\right)\right), \tag{19}$$

when a short circuit occurs, the ESR of the internal capacitor is maintained, in other words, the relevant column of the CB does not disconnect, but the voltage of the CB is distributed to the other capacitors of the relevant column capacitors, thus, the reliability relationship of the CB becomes as follows:

$$R_{\mathrm{CB,SC}} = \prod_{n=1}^{j}\left(1 - \prod_{m=1}^{i}\left(1 - R_{\mathrm{mn}}(t)\right)\right), \tag{20}$$

therefore, the reliability of the capacitor bank will be as in (21), shown at the bottom of the next page.

Substituting the R(t) obtained from Table 2 into (21) and considering the time from zero to 2×10^6, Figure 2 is obtained.

In the case of a fault, the voltage stress factor is modified according to the respective fault. With these interpretations, the reliability assessment also improves. Degradation occurs in both capacitance and ESR of the capacitors. Over time, capacitance decreases, and ESR increases. ESR plays no role in calculating reliability, but it does play a significant role in calculating the maximum power that a capacitance bank might provide. The peak output current supplied by the capacitor is calculated as follows [27]:

$$I_{\mathrm{peak}} = \frac{\frac{1}{2}V_R}{\frac{\Delta t}{C} + \mathrm{ESR_{DC}}} = \frac{1}{2}\frac{CV_R}{\Delta t + \mathrm{ESR_{DC}} \times C}. \tag{22}$$

Equation (22) confirms that the maximum current that CB can supply depends on the capacitance of C and ESR. Hence, the degradation of these two variables is very effective in determining the maximum current. The LSTM method is in charge of estimating and predicting the degradation of ESR and Capacitance after encountering a fault. The ESR of a capacitor is resistance and could be calculated using (23) in time [28]:

$$\mathrm{ESR}_t = \frac{\mathrm{ESR}_0}{\left(1 - k.t.\exp\left(\frac{-E}{T+273}\right)\right)}. \tag{23}$$

IV. PROPOSED ONLINE LSTM METHOD CONSIDERING FAULTS

In this paper, the LSTM has two main tasks:1) ESR and capacitance degradation forecasting of CB by considering sudden faults over real-time, and 2) fault detection in case of damage and problems in the analog fault detection system. A standard LSTM network unit comprises three principal cells: an input gate, a forget gate, and an output gate. To establish long-term time dependency, the LSTM determines and maintains the cell state to adjust the flow of information, which is a crucial criterion in the LSTM framework [16]. The state of the memory cell C_{t-1} intervenes with the intermediate output h_{t-1} and the subsequent input x_t to define which elements of the internal state vector need to be updated, maintained, or disappeared based on the outputs of the preceding time steps and the inputs of the current time step.

The gate processing options include a sigmoid network and bitwise multiplication. A sigmoid network can produce a value between 0 and 1, which specifies whether the input value can pass through a gate or not. The objective of the forget gate is to enable the LSTM network to forget earlier worthless information [16].

$$f_t = \sigma\left(W\left[x_t, h_{t-1}, C_{t-1}\right] + b_f\right). \tag{24}$$

The input gate function defines the present state C_t under the current input $[h_{t-1}; x_t; C_{t-1}]$ and C_{t-1}.

$$i_t = \sigma\left(W\left[x_t, h_{t-1}, C_{t-1}\right] + b_c\right), \tag{25}$$

$$C_t = f_t.C_{t-1} + i_1.\tanh\left(W\left[x_t, h_{t-1}, C_{t-1}\right] + b_c\right). \tag{26}$$

$$o_t = \sigma\left(W\left[x_t, h_{t-1}, C_t\right] + b_o\right), \tag{27}$$

$$h_t = \tanh(C_t).o_t \tag{28}$$

in which σ is a logical function with the outputs scaled to (0,1) [16].

A. THE PROPOSED LSTM RNN METHOD STRUCTURE

The RNN Deep learning method employed in this paper comprises three LSTM layers and a single dense layer, a Fully-connected layer. The LSTM conducts the ESR and

TABLE 3. Parameters of the proposed LSTM.

	Item	No.
1	epoch	100
2	batch size	1
3	learning rate	0.01
4	optimizer	Adam
5	LSTM layer	3
6	input shape	1

Capacitance forecast and fault detection of the proposed CB. Table 3 displays the LSTM network information. In neural network learning, sometimes, not entire input data is transferred. Input data is split into smaller same-size packets, and the information is sent in batch sizes. During network learning, the dropout accidentally releases some neurons. Due to the network architecture, an adequate dropout may result in proper learning.

Here, the LSTM operation is divided into two major components: fault-free mode and post-fault mode. In the case of no-fault, the LSTM continues to operate normally, and the dropout of the first and second layer is 50% and 40%, respectively, and in post-fault mode, the dropout is zero. Figure 3 shows the dropout of the proposed LSTM prediction method. This figure shows the reduction in processing when the dropout is taken into consideration. Optimizers represent the algorithms or approaches employed to modify neural network attributes to minimize losses. The optimizer used here is Adaptive Moment Estimation (Adam) [29].

In the proposed framework, a relationship was made between the predicted and actual data values using the evaluation criteria Max Error, MSE, RMSE, and MAPE, which are as follows [25]:

$$\text{MAPE} = \frac{1}{n}\sum_{i=1}^{n}\left|\frac{A_i - F_i}{A_i}\right| \times 100\% \quad (29)$$

$$\text{MSE} = \frac{1}{n}\sum_{i=1}^{n}(A_i - F_i)^2, \quad (30)$$

$$\text{RMSE} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(A_i - F_i)^2}, \quad (31)$$

$$\text{Max Error (ME)} = \underset{i}{\text{MAX}}\,|A_i - F_i| \quad (32)$$

The flowchart of the reliability and maximum current of CB prediction and fault detection using the online LSTM is presented in Figure 3(a). First, the voltages and currents are measured. Based on these parameters, the reliability and peak current of the CB can be measured, and the analog fault detection process can be started, as shown in Figure 3(b). Post-fault LSTM performance is different from pre-fault. After occurring the fault, the time for voltage sampling decreases, and the dropout becomes 0. Still, before the event of the fault, the voltage sampling increases, the data transferred to the LSTM are performed every 5 (h), and the dropouts of the first and second layers are 50% and 40%, respectively. The data is entered into the LSTM, the prediction process is executed, and finally, the feedback of the predicted data enters the fault process block to be compared with the actual data, as shown in Figure 3(b).

B. OFF-LINE LSTM

In this section, an initial test is conducted to validate the capacitor capacitance prediction by the LSTM method. The capacitance degradation of four parallel capacitors was recorded during 2000 (h) in a 13-level multilevel inverter [12]. In the previous section, the CB was used to validate the flowchart diagram of the improved fault detection method. These capacitors have been under voltage and current stress and tension for 2000 (h). To record the actual information, the capacitors were disassembled separately, and the capacitance of each capacitor was measured individually, and they were reassembled in the inverter.

To validate the LSTM prediction in its normal state, experimental tests were conducted on four real capacitors, and the forecast results of each capacitor were compared with the LSTM prediction. Figure 5 shows a comparison of the LSTM prediction and the actual measured capacitance. The LSTM outputs are ESR and Capacitance degradation predictions that were slightly different from the actual value, allowing them to be used in subsequent forecasts.

Figure 5 shows that as time increases, the capacitance of the capacitor decreases, and consequently, the output current supplied by the CB also decreases. The maximum output current is calculated according to Eq. 21 in $dt = 0.001$. Figure 6 also shows the effect of the ESR degradation over 2000 (h) on the output current of the CB. It is clear from the figure that the ESR increases over time, reducing the maximum output current of the CB.

C. ON-LINE (REAL-TIME) LSTM

When a fault occurs, the magnitude of the ESR and the capacitance suddenly increase or decrease. The magnitude of this

$$\begin{aligned} R_{\text{CB}} &= R_{\text{CB,OC}} + R_{\text{CB,SC}} - \left(R_{\text{CB,OC}} \times R_{\text{CB,SC}}\right) \\ &= \left\{ \begin{array}{l} \left(1 - \prod_{n=1}^{j}\left(1 - \prod_{m=1}^{i}\left(1 - R_{\text{mn}}(t)\right)\right)\right) + \left(\prod_{n=1}^{j}\left(1 - \prod_{m=1}^{i}\left(1 - R_{\text{mn}}(t)\right)\right)\right) - \\ \left[\left(1 - \prod_{n=1}^{j}\left(1 - \prod_{m=1}^{i}\left(1 - R_{\text{mn}}(t)\right)\right)\right) \times \left(\prod_{n=1}^{j}\left(1 - \prod_{m=1}^{i}\left(1 - R_{\text{mn}}(t)\right)\right)\right)\right] \end{array} \right\} \end{aligned} \quad (21)$$

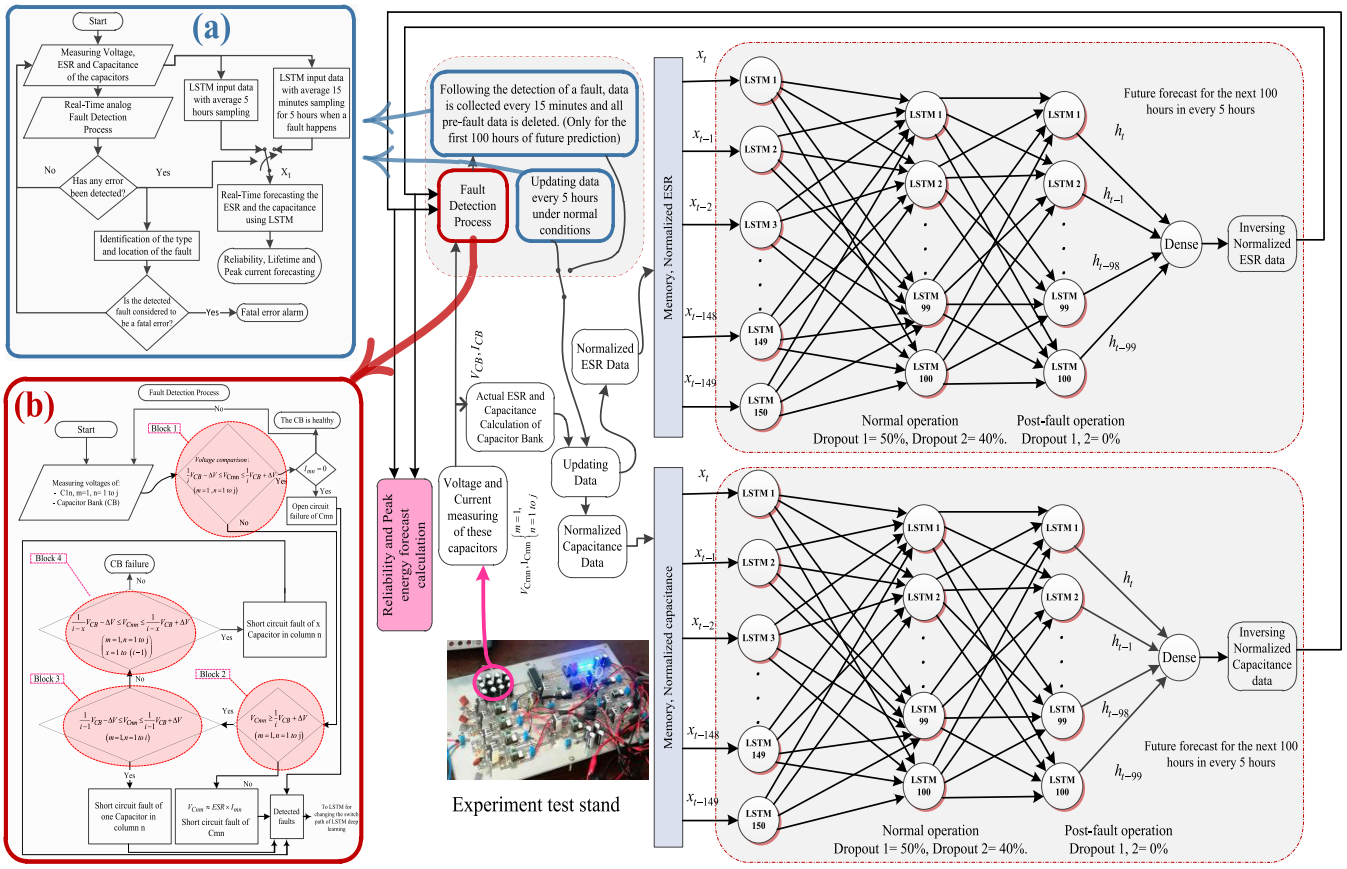

FIGURE 3. The reliability and peak current forecast diagram based on the LSTM, a) the reliability and peak CB current forecasting flowchart, b) Real-Time Fault detection flowchart of the capacitor bank.

FIGURE 4. Capacitors that were assembled and disassembled for measurement.

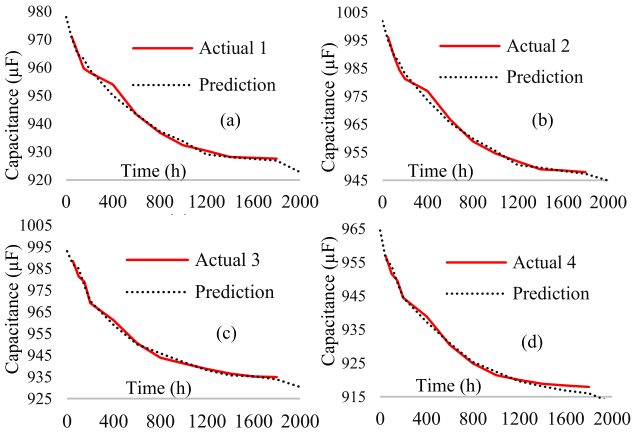

FIGURE 5. Comparison of LSTM capacitance predictions with actual values of capacitors with no fault encountered.

increase or decrease depends on the type and severity of the fault. Thus, after the failure, the data used for LSTM training deviated from the actual data. Therefore, it is necessary to update the data used by the LSTM. Figure 5 shows how the capacitance of the capacitors are derived and predicted by LSTM after degradation and fault.

As shown in Figure 7, until a fault happens, the LSTM uses the initial data of the previously tested capacitors as X_t input and switches to new real-time data as soon as the fault occurs. Since the first fault occurs, the LSTM no longer uses the initial data from the old capacitors and uses new input data. After each fault, all input data is cleared, and the latest current information is recorded, memorized, and used for prediction after the fault.

Using (24), the capacitance of the CB is measured and compared to the predicted output of LSTM [30]:

$$i_C = C_{(CB)} \frac{\mathrm{dV_{CB}}}{\mathrm{dt}} \Rightarrow C_{CB} = i_C \times \frac{\Delta t}{\Delta V_{CB}}. \quad (33)$$

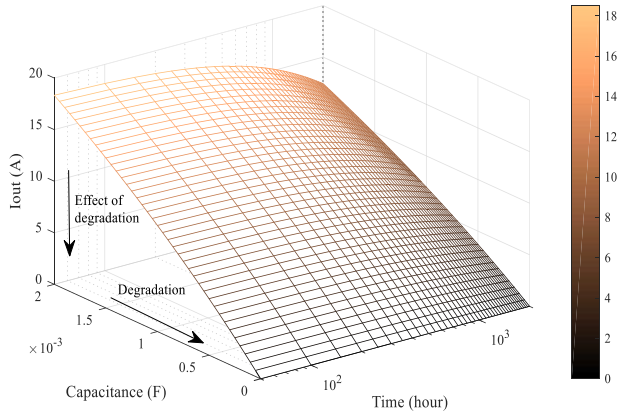

FIGURE 6. The effect of capacitance degradation on the output current of a capacitor bank during 2000 (h).

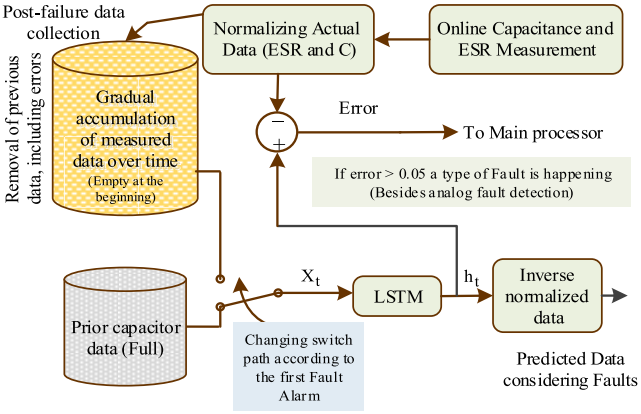

FIGURE 7. Real-time forecast diagram of ESR and capacitor factors after the fault.

The ESR of the capacitor is also calculated according to:

$$\tan\delta = \frac{\text{ESR}}{X_{C_d}} = 2\pi f C_d \text{ESR} \Rightarrow \text{ESR} = \frac{\tan\delta}{2\pi f C_d} \quad (34)$$

The tanδ changes with time. In [39], the tanδ changes were recorded during a 5-month endurance test, and the results show that the tanδ changes are less than 0.6%. Considering 1% of the measured capacitance difference, it seems that the presented method calculates the ESR value with less than 1.6% error. The value tanδ = 0.12 is given in the UVY1H102MHD1TO capacitor datasheet. Since the capacitor operates at a frequency of 100 Hz (two half cycles of 50 Hz) and, the capacitance is 1000 microfarads, for each capacitor, the value of ESR = 0.19 Ω. Thus, according to (25), the ESR of the CB in regular operation with no fault is equal to 0.1425 Ω. The LSTM forecasts the ESR and capacitance of the CB. The CB's reliability, lifetime, and peak output current are calculated from the artificial intelligence output data. Figure 8(a) and Figure 8(b) illustrate the capacitance and ESR prediction of the CB by taking into account all types of faults. Figure 8(a) illustrates the difference between the actual capacitance and the predicted capacitance by LSTM over 2000 (h). Figure 8(b), also shows the difference between

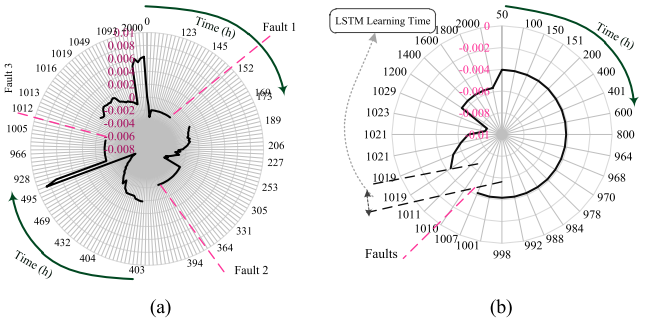

FIGURE 8. The difference between the actual and the predicted data: a) the difference between the actual capacitance and the predicted capacitance over 2000 (h), b) the difference between the actual ESR and the predicted ESR over 2000 (h).

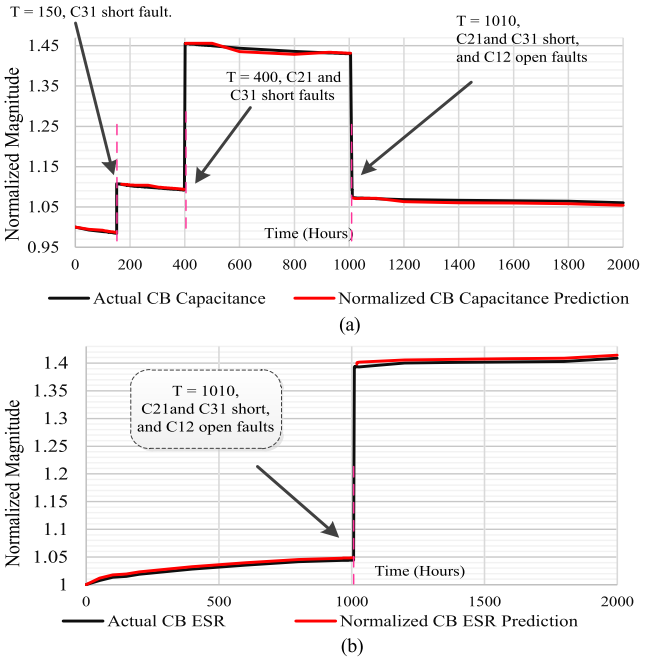

FIGURE 9. The CB parameters prediction: (a) the comparison of LSTM prediction and actual capacitance, (b) the comparison of LSTM prediction and actual ESR.

the actual ESR and the predicted ESR through the LSTM over 2000 (h). In these two figures, there are empty spaces on the screen; these spaces represent the first (h) after the fault in which the artificial intelligence is being trained. After the fault, the primary data is cleared and the LSTM training is performed using the new data.

Also, Figure 9(a) shows the comparison of LSTM prediction and actual capacitance. It also illustrates the effect of experimentally tested short circuit faults on the normalized capacitance. First C31 short circuit fault occurs at t = 151 h, subsequent C32 short circuit fault occurs at t = 400 h, and finally, C21 open-circuit fault occurs at t = 1010 h on the CB. The short circuit fault leads to an increase in capacitance, and the open-circuit fault leads to a decrease in capacitance of the CB. Figure 9(b) shows the comparison of LSTM prediction and actual ESR. It also displays the effect of the tested faults

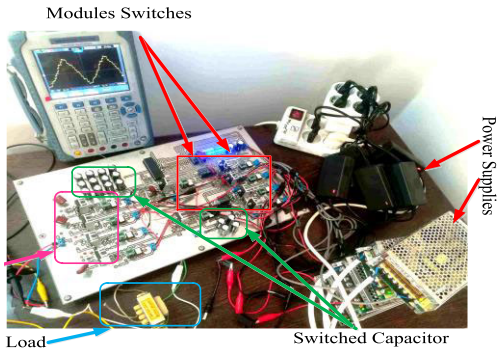

FIGURE 10. The prototype configuration of the multi-level inverter.

on the ESR of the CB. It can be argued that the ESR resistance does not change with a short-circuit fault of the capacitor. But with an open-circuit fault, the whole column of capacitors disconnects. With an open-circuit fault of the capacitor, the ESR of the CB increases, which means a decrease in the current drawn from the CB.

V. EXPERIMENTAL RESULTS AND DISCUSSION

A. FAULT DETECTION

A CB consisting of 12 capacitors was used on a smaller scale to validate the indicated content. Figure 10 shows the multilevel inverter that was used for the test [12]. The arrangement of the capacitors is shown in Figure 1(b). UVY1H102MHD1TO is the part number of 12 capacitors in the experimental test. Figure 11(a) shows the voltages V_{CB} and V_{C11} of the inverter in regular operation without fault. This CB in the 13-level inverter is a type of switched capacitor.

The short circuit in the experimental setup is implemented using a wire across the related capacitors. In preparation for the open circuit test, one of the capacitors was disconnected from the board, and the pins were connected to the board with two wires. Then the capacitor was disconnected by cutting one of the wires.

The worst-case scenario that can happen to the CB's internal capacitors is the simultaneous short circuit of several capacitors because the voltage of the capacitor bank is distributed among the remaining series capacitors of the relevant column. Note that if the applied voltage is higher than the capacitor's rated voltage, the capacitor explodes.

To sense each capacitor voltage, an ADC pin of the processor is assigned, then the voltage is measured continuously, and the processor reads the data steadily.

The voltage is measured instantaneously and the comparison is made instantaneously. In other words, we don't wait until the capacitor's voltage peak is reached before measuring and comparing the voltages of the first capacitor (in this case, capacitor C11) and VCB.

To perform the experimental tests, four scenarios are examined, including all possible faults on one CB's column which are C31 short circuit, simultaneous C21 and C31 short circuits, C11 open circuit, and C31 open circuit. In the following, the different scenarios are described:

1) SCENARIO NO. 1: OCCURRENCE OF A SHORT-CIRCUIT FAULT IN ONE OF THE INTERNAL CAPACITORS

The first scenario is when the capacitor C31 is short-circuited. The voltage of each capacitor before the short circuit is $V_{CB}/3$, but when one capacitor is shorted, the voltage of the other two capacitors becomes $V_{CB}/2$. Following this fault, the voltage across capacitor C11 increases from a peak of 8 volts to a peak of 12 volts. According to the fault detection flowchart shown in Figure 3(b), a fault is detected in block 3 for $i = 3$. A short-circuit fault in one capacitor of a column causes the voltage of the capacitor bank to be distributed to other capacitors. By inserting the approximate value of the voltages at the fault point, (35) can be represented. Figure 11(b) shows is related to this scenario.

$$\left\{\tfrac{1}{2}V_{CB} - 1 \le V_{C11} \le \tfrac{1}{2}V_{CB} + 1 \Rightarrow V_{CB} \approx 19.5, V_{C11} \approx 9 \right. \\ \Rightarrow \{8.75 \le V_{C11} \approx 9 \le 10.75 \tag{35}$$

2) SCENARIO NO. 2: THE OCCURRENCE OF A SIMULTANEOUS SHORT-CIRCUIT FAULT OF TWO INTERNAL CAPACITORS IN ONE COLUMN

The second scenario is the simultaneous short circuit of two capacitors C_{31} and C_{21}. Before the short circuit, the voltage on each capacitor is $V_{CB}/3$, but when these two capacitors are shorted, the voltage of the remaining capacitor becomes V_{CB}. Figure 11(c) illustrates the voltage of capacitor C_{11} when C_{21} and C_{31} are shorted simultaneously. Each column has three capacitors; shorting these two capacitors makes the voltage C_{11} equal to the voltage of the capacitor bank. Detecting this fault is the task of block 4 of the flowchart shown in Figure3(b). Note that the output x of block 4 is equal to *2* (x=*2*).

$$\begin{cases} \frac{1}{i-x}V_{CB} - \Delta V \le V_{Cnm} \le \frac{1}{i-x}V_{CB} + \Delta V \\ \begin{pmatrix} m = 1, n = 1 \; to \; \mathrm{j} \\ x = 1 \; to \; (i-1) \end{pmatrix} \end{cases}$$

$$\Rightarrow \begin{cases} i & = 3 \\ x & = 2 \\ \Delta V & = 1 \end{cases} \tag{36}$$

$$V_{CB} - 1 \le V_{C11} \approx V_{\mathrm{CB}} \le V_{CB} + 1 \tag{37}$$

Due to equations (36) and (37), it is evident that the voltage is in the specific range determined by block 4. The nominal voltage of the capacitor selected for testing is 50 volts, which means that if two of the three capacitors in the column are short-circuited, the capacitors' nominal voltage is still higher than the applied voltage. However, sometimes when a short-circuit fault occurs, the applied voltage is higher than the nominal voltage. In this case, the algorithm should issue a quick command to disconnect from the system and discharge the energy of the capacitor bank.

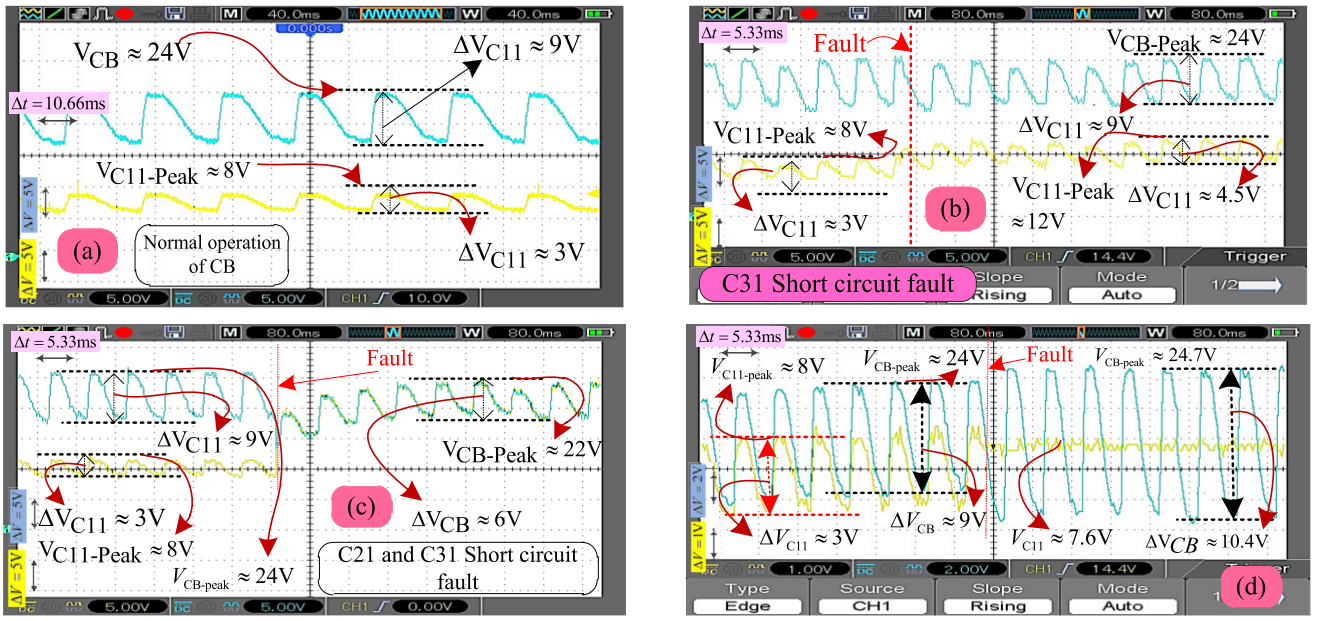

FIGURE 11. The result of the experimental prototype: (a) C11 and VCB voltages in the normal operating mode without fault, (b) the effect of C31 short circuit fault, (c) the effect of simultaneous short circuit faults of C21 and C31, increase in capacitance leads to decrease in voltage fluctuations, and (d) the effect of C12 open circuit fault, as a result of the noticeable reduction in capacitance of the capacitance bank, the voltage fluctuation increases.

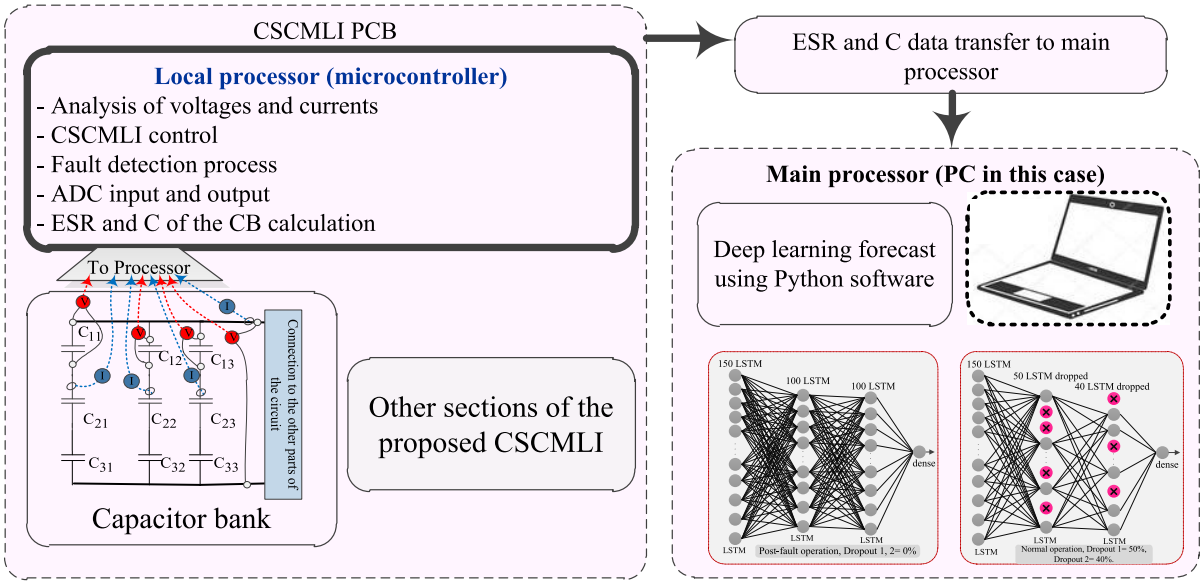

FIGURE 12. Topology corresponding to the experimental platform.

3) SCENARIO NO. 3: THE OCCURRENCE OF AN OPEN-CIRCUIT FAULT OF AN INTERNAL CAPACITOR

In this scenario, an open-circuit fault occurs for capacitor C12. It is worth noting that the open-circuit fault of one, two, or more capacitors make no difference from the standpoint of the presented method because the same open-circuit fault in an internal capacitor leads to the disconnection of the entire corresponding series capacitors. By breaking the connection, the remaining capacitors do not discharge quickly, so their voltage remains constant for a while (the time during which the fault detection process operates is referred to as constant here) and slowly discharges. The capacitor's constant voltage is depicted in Figure 11(d) along with the voltage sampling results. Immediately after an open-circuit fault occurs, the capacitor voltage remains constant at the voltage it had and does not fluctuate. In this case, the output current of this column is zero; this fault is detected in block 1. Equations(38) and (39) illustrate the related calculations. However, the most

obvious sign of a short-circuit fault is the zero amperes of output current flowing through the column. Even without the need for block 1 relationships, the occurrence of a short-circuit fault can be detected if it is specified that the output current of the column is zero.

$$\begin{cases} \frac{1}{i}V_{CB} - \Delta V \le V_{\mathrm{Cmn}} \le \frac{1}{i}V_{CB} + \Delta V \\ (m = 1, n = 1 \; to \; \mathrm{j}) \end{cases}$$

$$\Rightarrow \begin{cases} i = 3, \\ m = 1, \\ n = 1, \\ \Delta V = 1 \end{cases}, \begin{cases} V_{\mathrm{CB}} \approx 20.5 \\ V_{\mathrm{C11}} \approx 7.6 \end{cases} \tag{38}$$

$$\begin{cases} \frac{1}{3}V_{CB} - 1 \le V_{\mathrm{C11}} \le \frac{1}{3}V_{CB} + 1 \\ (m = 1, n = 1 \; to \; \mathrm{j}) \end{cases}$$

$$\Rightarrow \begin{cases} i = 3, \\ m = 1, \\ n = 1, \\ \Delta V = 1 \end{cases} \begin{cases} 5.83 \le 7.6 \le 7.83, \\ I_{11} = 0. \end{cases} \tag{39}$$

An increase in the voltage ripple of the capacitor bank is another sign of an open-circuit fault. The voltage ripple increases as the energy demanded by the mains/system remain constant, according to equation (40).

The occurrence of an open-circuit fault can be detected based on this increase in voltage ripple, but to ensure the occurrence of a fault, the current of each column is measured. Figure 11(d) depicts the rise in CB voltage ripple following the fault.

$$I_C = C\frac{dv}{dt} \Rightarrow dv = \frac{I_C \times dt}{C} \tag{40}$$

4) SCENARIO NO. 4: TWO CAPACITORS OPEN CIRCUIT FAULTS AT THE SAME TIME

In this scenario, an open circuit fault occurs on two capacitors C21 and C31 at the same time. Because of the open circuit, the results of this scenario are similar to scenario number 3 because the occurrence of an open circuit on one capacitor does not differ from the occurrence on two capacitors at the same time, and the results are the same.

B. ADAPTION OF THE FAULT DETECTION METHOD AND LSTM PREDICTION TECHNIQUE

The topology corresponding to the experimental platform is shown in Figure 12. In the proposed manuscripts, the fault detection is implemented in the local processor, the AVR microcontroller. Then, the ESR and capacitance data of the capacitor bank are transferred to the main processor, here the PC. The real-time forecasting considering the faults is accomplished on the PC using Python software. The results of the previous section figures show that the short-circuit fault leads to an increase in capacitance, the ESR does not change and the CB current increases, and the open-circuit fault increases the ESR, decreasing the current and the capacitance. Short-circuit fault leads to a severe momentary drop in reliability and completely drops the entire reliability curve,

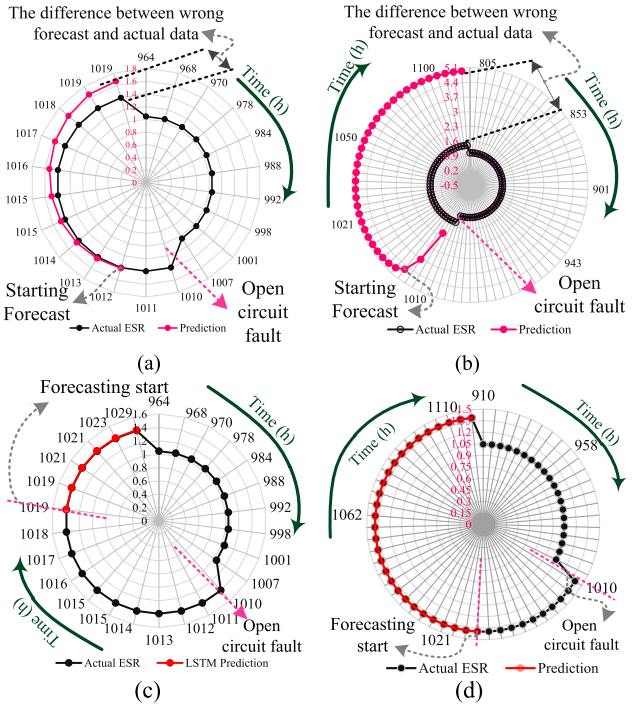

FIGURE 13. The low post-failure and input data of the LSTM. a) low post-failure data lead to erroneous predictions, ESR predictions, b) input data of the LSTM, two post-failure data, and 100 (h) pre-failure data, c) input data of the LSTM, 10 post-failure data, d) input data of the LSTM, 10 post-failure data, and 100 (h) pre-failure data, In the 100 (h) that the LSTM predicts.

and open-circuit fault slightly increases reliability. Following Eq. 8, a reduction in capacitance leads to a reduction in the capacitance factor, which increases the reliability of the capacitor.

When a fault occurs, several problems arise: 1) the fault that occurred suddenly is irrelevant to the internal structure of the capacitor, and this fault may not occur again, so the data should not be used for training, 2) with the average of every 5-(h), it takes a long time for the LSTM to be able to make accurate predictions. 3) the LSTM needs to be instructed not to use pre-failure data. But the biggest challenge is that the LSTM needs a minimum of training data to make a correct forecast.

To overcome these challenges, as shown in Figure 3, the first thing to do after the fault occurs is two actions: 1) the data previously used for fault-free capacitors for the LSTM input should no longer be used, and new data switched, i.e., the health data of capacitors completely is deleted and new update data used, and 2) after a fault occurs, instead of 5 (h) on average, input data is added to the LSTM approximately every 15-(min) until the correct prediction is made and the difference from the actual value is minimized. The following figures show how prediction goes wrong with insufficient data.

In Figure 13(a), two post-failure data and ten pre-failure data are given to the LSTM to predict the next 10-(h), where the markers are data indicated in the figure. After the fault,

TABLE 4. Capacitor monitoring and fault detection comparison between similar approaches and the proposed technique.

	Application of the CB	Fault type detection ability	Fault detection/ monitoring method	Experimental / simulation	Advantages and disadvantages
[53]	Transmission line	Short circuit	An algorithm based on discrete wavelet transform (DWT)	Simulation using PSCAD software	+ High accuracy (100%), fast fault detection. - Cannot identify the exact location of the fault.
[54]	Transmission line	Short circuit	An algorithm based on discrete wavelet transform (DWT)	Simulation using PSCAD/EMTDC software	+ Fast fault detection, prevention of unbalanced current protection relay, fast fault detection, the ability to recognize fault and inrush current. - Require a high-performance PC to shorten the operating time.
[55]	Electric vehicle	Open circuit	A synthetic design of Luenberger observers and learning observers	MATLAB and experimental setup	+ High accuracy. - Unable to detect short circuit fault, the complexity of the fault detection method.
[56]	Electric vehicle, marine	Open circuit	Evidence reasoning and backpropagation neural network	MATLAB simulation using experimental learning data	+ High accuracy. - Training the neural network requires a large amount of time and data, ignoring short circuit fault of the capacitors.
[57]	Electric vehicle - DC-DC & DC-AC	Short circuit Open circuit	Short-time Fourier transform	Experimental test	+ Simplicity and inductance-independency, easily applied in both dc–dc and ac–dc conversions, estimation accuracy almost equal to 6%. - Additional sensor required.
[58]	Solar system	Open circuit	Combination of the new analog approach with MPPT.	Experimental test	+ No additional current or voltage sensor is required, simple fault detection procedure. - The possibility of incorrect measurement due to noise caused by switching, requires a high sampling rate.
[59]	PFC converter	Short circuit Open circuit	Non-invasive online monitoring Method	Experimental test	+ High accuracy, no additional current or voltage sensor is required. - Dependence on the inductance of the load and the converter, accurate measurement required.
[60]	Flyback converter	Short circuit Open circuit	Non-invasive online monitoring Method	Experimental test	+ Non-invasive measurement, high accuracy. - Dependence on the inductance of the load and the converter, accurate measurement required.
[61]	DC link converters specially PV	Short circuit Open circuit	Condition monitoring	Overview including experimental and simulation	+ High accuracy, fast. - Accurate measurement required.
[62]	DC-DC renewable systems	Short circuit Open circuit	Walsh–Hadamard transformation and recursive least square based on a state-space model with full-state observation	Experimental test	+ Low sampling rate, no additional current or voltage sensor is required, good accuracy. - The complexity of the monitoring and in result, complex fault detection method, dependence on the inductance of the load and the converter.
[63]	Flyback converter	Short circuit Open circuit	Non-invasive online condition monitoring	Experimental test	+ No additional current or voltage sensor is required, easy and simple to implement. - Noise and voltage spikes during switching can increase the probability of errors during amplification.
[64]	Uninterrupted Power Supplies	Open circuit (wear out)	Real-time condition monitoring and a predictive-maintenance	Experimental test	+ No additional current or voltage sensor is required, easy, cheap and simple to implement. - Accuracy of about 10% or less, unable to detect the type of internal capacitor fault.
[65]	DC-AC solar inverter	Short circuit Open circuit	Online health monitoring of AEC.	Experimental test	+ High accuracy, design is based on IEEE 929-2000 standard, easy and simple to implement. - Small signal injection circuit, not considering capacitance degradation.
Pro. article	All DC links of Electric vehicle	Short circuit Open circuit	Online monitoring and fault detection. Lifetime prediction.	Experimental test	+ Accurate sensing of current and voltage is not required (Inexpensive sensors are sufficient), fast internal fault detection, non-invasive measurement, able to detect sudden faults and predict normal faults, high accuracy. - Additional sensor required; the deep Learning implementation requires a PC to use the Python software for prediction.

the command is sent through the processor, and instead of averaging data for every 5-(h), data is sent to the LSTM every 15-(min) to increase the accuracy of the prediction. The prediction deviates from the true value because the entirety of the learning data is insufficient, i.e., more data is needed after the fault occurrence. The purpose of showing this figure was to validate the fact that more data is required to make accurate predictions. Now the data of pre-failure is added to observe the result of the prediction. Figure 13(c) shows the ESR prediction for the next ten (h) by the LSTM with input data from ten (h) before the failure and ten data after the failure. At t = 1010 (h), the C21 open-circuit fault occurs. As it can be seen, the difference between the predicted and actual data is quite small. The result shows that with the LSTM parameters set, in ten (h) of the pre-faults and ten post-fault data input and training, the prediction is highly satisfactory. Note that the pre-fault data is learned to the LSTM on average every 5 (h) and post-fault data is learned every 15 (min) on average. Hence, ten post-fault data correspond to 150 (min) or two (h) and 30 (min) (less than half the time of one of the pre-fault data). Figure 13(d) shows the prediction of the next 100 (h) of ESR by the LSTM artificial intelligence method with ten post-fault data and one hundred (h) of pre-fault data. The difference between the prediction and the actual is insignificant. The result depicts only ten data (about 150 (min)) after the fault, and one hundred (h) before the fault

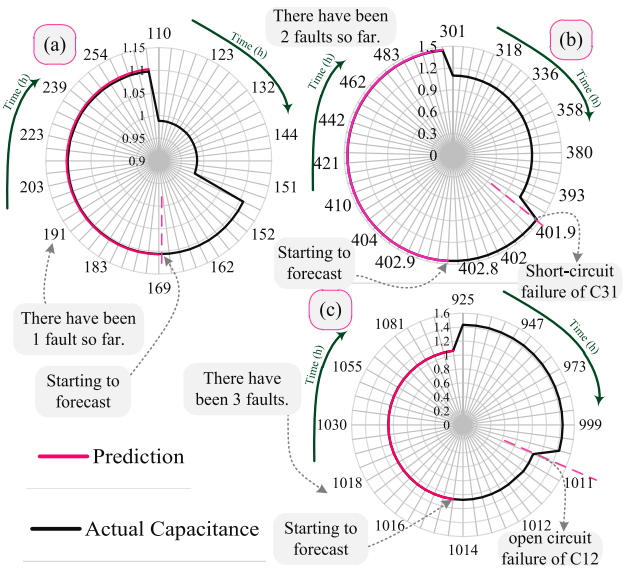

FIGURE 14. Post-Fault forecast of the next 100 (h) of CB capacitance, a) The first sudden short-circuit failure of C31 at t=150 (h), b) The second sudden short-circuit failures of C21 at t=150, and C31 at t=400 (h), c) Short-circuit failures of C21 and C31, and open circuit failure of C12 in t=1010 (h).

are sufficient to make a fairly accurate prediction of the next 100 (h) data.

TABLE 5. Proposed LSTM method comparison with similar deep learning methods.

	Method	Best score	application	Based on
[42]	LSTNet, TPA-LSTM, DA-RNN	RMSE : 11.6477	Wind Power Forecasting	RNN
[43]	Attention LSTM	RMSE=1.52, MAE = 1.17	(RUL) of BLDC motor affected by different stator faults	RNN
[44]	BIGRU	RMSE = 6,75, MAE = 4.10	Wind Power Prediction	RNN
[45]	VMD–GRU	CWC = 1.3663	Short-Term Wind Power Interval Prediction	RNN
[46]	CNN-GRU	17.01 MAPE	Predicting Wind Power	CNN-RNN
[47]	Improved Deep Mixture Density, Network	MAE = 6,88%, RMSE = 9,38%	Wind Power Probabilistic Forecasting	MDN
[48]	BILSTM	MSE = 1.1251, MAE = 2.4540, MAPE = 9.4041	One-Hour-Ahead Wind Power Forecasting	RNN
[49]	KK-CNN-GRU	RMSE =168, MAPE = 12.0	Multi-Step Ahead Wind Power Predictions	CNN-RNN
[50]	GRU	MAPE=0.8708, RMSE = 1.0411 2	Wind Speed Forecasting	RNN
[51]	PCA-LSTM	MAE = 7,787, RMSE = 10.431, MAPE =4.448	Wind Power Prediction	RNN
[52]	WT-CNN	RMSE=0.20%	Short-Term Wind Power Prediction	CNN
Proposed	LSTM	MSE=0.00058, RMSE=0.024, MAPE=0.015, Max Error=3.23%	Capacitor Bank lifetime prediction considering internal faults	RNN

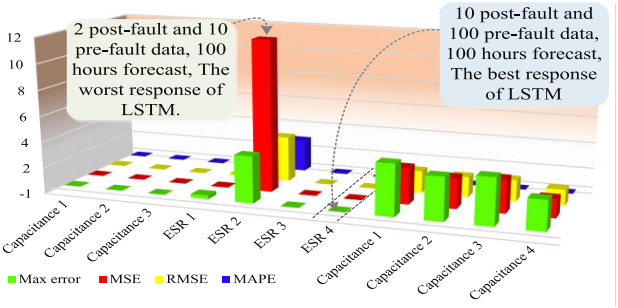

FIGURE 15. Comparison of error criteria results with different post-fault data.

Figure 14 shows the prediction of capacitance by the LSTM for the next 100 (h) with ten data after the fault, and 100 (h) of data before the fault as its input. The figures show that although the most difficult case with little data (ten data after the fault) is given as input to the LSTM, the prediction is relatively acceptable.

The largest MAPE difference is observed in item 3, where the input data for the LSTM consists of two post-fault data and 10 (h) of data before the fault occurs, and the forecast is made for the next 100 (h). The result shows that the LSTM with low learning input data produces inaccurate predictions. Figure 15 depicts a comparison of error criteria results with different post-fault data. It is clear from the figure that the worst response of the LSTM is the ESR prediction after error as well as low post-fault data. With the proposed method, the voltage sampling time is reduced from 5 (h) to 15 (min) immediately after the fault occurrence, and this data is considered input data for the LSTM.

After the initial forecasting is performed, the LSTM repeats a separate forecast every 5 (h) for low MAPE. As long as no fault occurs, no continuous operation of the processor is required. After the fault detection, the LSTM input data is modified, and the forecasting begins using new input data. Using the proposed method, instead of 15 (min) of post-fault sampling, it is possible to sample the required parameters even every one second and allow the LSTM to predict much faster. A trade-off between system performance, processor performance prioritization, and prediction intensity is established. So, the input data sampling for the LSTM needs to be determined based on overall system performance.

Table 4 illustrates the comparison between the proposed analog fault detection method and other similar methods, and Table 5 shows the comparison of the applied LSTM method with similar deep learning methods used for prediction. As shown in these tables, the advantages of the proposed combined methods are: accurate sensing of current and voltage is not required (Inexpensive sensors are sufficient), fast internal fault detection, non-invasive measurement, ability to detect sudden faults and predict normal faults, high accuracy and, the disadvantages are: additional sensor required and the LSTM deep learning implementation requires a PC to use the Python software for prediction.

VI. CONCLUSION

Sudden faults can damage the internal capacitors of the CB. These damages may include short-circuit and open-circuit faults of the internal capacitors, which change the capacitance and ESR of the CB. In addition, the ESR and capacitance of capacitors are degraded over time. Capacitor degradation reduces the energy storage factors, capacitor current, reliability, and system lifetime. In this paper, the LSTM artificial intelligence method is used to forecast the degradation of capacitor parameters. By using the obtained results, the reliability and peak output current of the CB is predicted. The effect of fault types on capacitor parameters is investigated, and the adverse impact on the predictions is presented. The post-failure challenges of the accurate forecast of the LSTM are also examined, and solutions are provided. A method based on the measurement of voltage and current changes is used to detect sudden faults, and an algorithm for fault detection is proposed. The proposed method enables the identification of the type and approximate location of the fault of each capacitor array in the CB. The fault detection results served an essential purpose in modifying the input data for the LSTM learning.

In this paper, two experimental tests were conducted. Four capacitors were loaded for 2000 (h) in the first test, and their degradation was recorded. The recorded data was used as the primary data required for the LSTM Deep learning, and the LSTM validated the accurate prediction of the degradation of capacitor parameters. Then, in the second test, in a CB composed of 12 capacitors in four columns, different types of short circuit and open circuit faults were applied, and the

proper operation of the detection method was demonstrated. The actual results and prediction of the parameters of the capacitance bank validated the correct process of the proposed novel method based on artificial intelligence LSTM deep learning. Finally, based on the final results and considering the faults, the CB's reliability and the peak current are predicted.

As shown in Table 4 and Table 5, the advantages of the proposed combined methods are: accurate sensing of current [31] and voltage is not required (Inexpensive sensors are sufficient), fast internal fault detection, non-invasive measurement, able to detect sudden faults and predict normal faults, high accuracy, and, the disadvantages are: additional sensor required and the LSTM deep learning implementation requires a PC to use the Python software for prediction.

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