6G4All: An Open SDR Platform on a Commercial Baseband SoC with OpenAirInterface for 6G Research and Deployment

Eric Mittag* , Lukas Brechtel* , Maximilian Stark† , Andrew Back‡ , Robert Schmidt§ ,
Hans D. Schotten*¶
*German Research Center for Artificial Intelligence (DFKI), Kaiserslautern, Germany
†CTO System Innovation, NXP Semiconductors, Hamburg, Germany
‡Lime Microsystems, London, United Kingdom
§OpenAirInterface Software Alliance (OSA), Biot, France
¶RPTU University Kaiserslautern-Landau, Germany

***Abstract*—Experimental 5G and 6G research is dominated by FPGA-based SDR platforms that impose prohibitive cost, require specialised hardware expertise, and create a transfer gap between research prototypes and commercial deployments. We present the 6G4All SDR platform—a compact PCIe module combining the NXP LA9310 commercial cellular baseband SoC with the Lime Microsystems LMS7002M RF transceiver—integrated into the 3GPP-conformant OpenAirInterface (OAI) 5G NR stack. The complete platform stack is open-source: hardware design files, VSPA DSP firmware, Lime Suite NG driver, and the OAI protocol stack. Target applications include RedCap-class UE and embedded edge deployments—drones, vehicles, robots—incompatible with rack-mounted FPGA hardware. We demonstrate end-to-end IP connectivity in SA mode across two FR1 bands and both duplexing modes: Band 5 (FDD, 20 MHz, 88.1 Mbit/s downlink with a COTS UE over the air) and Band 41 (TDD, attach and latency demonstrated), on two heterogeneous host ISA families. To our knowledge, this is the first experimental validation of standards-compatible 5G NR operation on a production-grade cellular baseband SoC with a commercial UE, closing the gap between open research and commercial deployment.**

***Index Terms*—software-defined radio, 5G New Radio, OpenAirInterface, baseband system-on-chip, NR RedCap, open-source hardware, LimeSDR, 6G**

PREPRINT
Accepted at IEEE PIMRC 2026.

I. Introduction

The global research community is accelerating its efforts towards 6G systems, with standardization activities expected to commence within the 3GPP Release 21 timeframe [1]. Experimental validation on physical hardware platforms is indispensable for this process. Yet the landscape of available SDR platforms presents researchers with an uncomfortable choice: entry-level devices that lack the bandwidth and processing capabilities required for 5G NR and beyond, or high-end FPGA-based systems that impose prohibitive costs and development complexity. Beyond cost, FPGA-based research results cannot transfer directly to products: the underlying hardware differs from production-grade silicon, forcing re-engineering and diluting R&D efficiency—a *transfer gap* that is rarely discussed.

Current experimental 6G research is dominated by FPGA-centric SDR platforms such as the Ettus/NI USRP and Xilinx RFSoC evaluation boards [2], [3]. For many universities, small and medium enterprises, and startups—particularly in regions with limited research budgets—these platforms remain out of reach.

To our knowledge, no existing platform simultaneously offers (a) sub-$300 affordability, (b) a commercial baseband SoC enabling direct technology transfer, (c) integration with a 3GPP-conformant open-source stack, and (d) open-source, software-programmable on-chip DSP acceleration on production silicon. The 6G4All initiative [4] addresses this gap with open, standards-compatible E2E solutions on commercial hardware, spanning terminal through RAN to core. This paper presents the RAN building block.

Specifically, we present the 6G4All SDR platform and make the following contributions:

1) A modular SDR architecture realized as the LimeSDR Micro—a compact PCIe module combining the NXP LA9310 commercial baseband processor, featuring integrated DSP acceleration for PHY-layer processing in a single-digit-watt power envelope, with the Lime Microsystems LMS7002M RF transceiver—deployable across a range of host platforms from embedded edge devices to high-performance servers [5].
2) Integration of this platform into the 3GPP-conformant OAI 5G NR stack [6], providing a complete open-source gNB and UE implementation.
3) E2E experimental validation across two FR1 bands

TABLE I
CLASSIFICATION OF CURRENT SDR PLATFORMS.

Tier	Examples	Bandwidth	Price	Target
Entry	RTL-SDR, ADALM-Pluto	$<$10 MHz	50 $ to 300 $	Education, hobby
Mid	LimeSDR, BladeRF 2.0	10 MHz to 60 MHz	250 $ to 500 $	Research, prototyping
High	USRP B210, RFSoC	100 MHz to 400 MHz	1400 $ to 30 000 $+	Industry, large labs

(FDD Band 5, TDD Band 41) and two host instruction set architectur families, demonstrating IP connectivity on a commercial cellular baseband SoC for the first time.

II. SDR LANDSCAPE AND THE FPGA PROBLEM

Since Mitola's foundational work on software radio architectures [7] and the emergence of GNU Radio as an open-source signal processing toolkit [8], SDR platforms have evolved from military research programs into a broad spectrum of commercially available systems. Today, these platforms can be grouped into three distinct performance tiers (Table I), each targeting different communities and use cases—yet none simultaneously satisfies the requirements of affordability, openness, and transfer readiness that 6G research demands.

A. Current SDR Platform Tiers

Entry-level devices such as the RTL-SDR dongle [9] or ADALM-Pluto [10] provide an accessible starting point for education and hobbyist experimentation, but their limited instantaneous bandwidth, frequency range and processing capabilities preclude 5G NR operation. Mid-range and higher-end LimeSDR platforms—including the LimeSDR XTRX and the LimeSDR X3, which supports 5G operation at 100 MHz 2T2R [11]—have demonstrated that host-side PHY processing can meet 3GPP requirements for base station applications. However, these platforms delegate all baseband computation to the host CPU, which limits their applicability in size-, weight-, power-, and cost-constrained (SWaP-C) deployment scenarios—most critically on the UE side, where dedicated baseband processing is essential and host-class compute resources are unavailable. The LimeSDR Micro presented in section III extends this philosophy by replacing the FPGA used in previous designs with an NXP LA9310 baseband processor and adopting PCIe for host communication—targeting software-programmable, and SWaP-C-optimized SDR operation with particular emphasis on UE-side and embedded applications. Platforms based on FPGAs—most notably the Ettus/NI USRP B210 [12] and Xilinx/AMD RFSoC evaluation boards [3]—deliver the bandwidth and processing power needed for 5G NR and beyond, but at costs that start at 1400 $ (for 61.44 MS/s) and routinely exceed 15 000 $ per unit. It is these platforms that dominate current 6G experimentation—and that impose the bottleneck described next.

B. The FPGA Bottleneck

Beyond cost, FPGA-centric platforms impose three structural problems. First, implementing and modifying PHY processing requires specialized hardware description language expertise and vendor toolchains, with iteration cycles measured in weeks rather than hours. Second, FPGAs are a poor architectural match for 5G PHY: the dominant operations—FFT/iFFT, LDPC, channel estimation—are narrow arithmetic kernels that FPGA logic implements at approximately $12\times$ the dynamic power and $40\times$ the die area of ASIC equivalents [13], directly driving the cost gap in Table I. Third, and most critically, FPGA-based results cannot transfer directly to products: re-engineering for production silicon creates a *transfer gap* where R&D investment is partially lost. Alternative approaches—closed-source x86 software stacks (e.g., Amarisoft [14]), GPU-based virtualized Radio Access Network (vRAN) (NVIDIA Aerial [15]), and look-aside LDPC accelerators [16], [17]—each eliminate part of the FPGA dependency but remain proprietary, cost-intensive, or unsuitable for embedded deployment.

III. THE 6G4ALL PLATFORM

The 6G4All SDR platform is realized as the LimeSDR Micro: a compact PCIe module designed by Lime Microsystems, integrating the NXP LA9310 commercial baseband SoC and the LMS7002M RF transceiver on a single PCB [5]. The LimeSDR Micro is the latest addition to the LimeSDR family—an open line of SDR boards where the complete PCB design and manufacturing data, firmware, and host software drivers are published under liberal open-source licensing with the objective of democratizing access to mid-range and higher-end SDR technology. By combining the LMS7002M transceiver with fully open-source hardware and software at a fraction of established alternatives' cost, the product line has attracted tens of thousands of users across research, education, and commercial prototyping [18]. By replacing the FPGA used in previous LimeSDR designs with the NXP LA9310 baseband processor, the LimeSDR Micro provides an all-software-programmable solution with integrated DSP acceleration, further lowering the barrier to experimentation. The presence of production-grade cellular silicon—rather than an FPGA—places the platform in a fundamentally different architectural category from high-end research SDRs.

A. Modular Platform Architecture

Figure 1 illustrates the overall system architecture. The platform comprises three main components: a *host platform* executing the upper-layer software stack, the *LimeSDR Micro* PCIe module providing baseband processing and RF functions, and the *PCIe interconnect* linking them. On the module, the NXP LA9310 baseband SoC and the Lime Microsystems LMS7002M RF transceiver share a single PCB. Host-side software accesses the platform through the Lime Suite NG open-source driver library [19], which abstracts RF control and I/Q streaming across all supported host platforms.

TABLE II
HOST PLATFORMS UNDER EVALUATION

Host SoC	Architecture	Cores	RAM
NXP LX2160A	ARMv8-A	16× A72	16 GB
NXP i.MX95	ARMv8.2-A	6×A55	8 GB
AMD Ryzen 9 7950X	x86 (Zen 4)	16×Zen 4	32 GB DDR5

The PCIe form factor decouples the SDR module from the compute environment, allowing the same hardware to operate across heterogeneous host platforms. To validate this portability, the platform was integrated and tested on three hosts spanning two instruction set architecture families: an ARMv8-A system (NXP LX2160A, 16×Cortex-A72), an ARMv8.2-A system (NXP i.MX95, 6×Cortex-A55), and an x86 system (AMD Ryzen 9 7950X, Table II). All three run the same OAI 5G NR build without platform-specific modifications. The LX2160A and Ryzen 9 meet the OAI minimum of 2×2 GHz CPU and 4 GB RAM [20]; the i.MX95 Cortex-A55 cores run at 1.8 GHz, below this threshold, making it the primary target for the PHY offload roadmap described in Section VII.

B. NXP LA9310 Baseband SoC

The NXP LA9310 is a commercial cellular baseband SoC from NXP's small-cell and radio-processing portfolio, designed for low-power, embedded, and cost-sensitive radio platforms. Beyond conventional baseband workloads, it targets embedded radio applications including RedCap-class UE front-ends [21], [22], reflecting a silicon architecture optimized for efficient embedded radio processing rather than general-purpose programmable logic.

As shown in Fig. 1, the LA9310 integrates a Vector Signal Processing Accelerator (VSPA) DSP subsystem, an ARM Cortex-A53 control processor, and a unified on-chip memory map. The VSPA DSP cores implement vectorized arithmetic pipelines optimized for PHY-layer processing such as FFT/iFFT, filtering, channel estimation, and channel coding. A defining characteristic of the architecture is its fully software-programmable nature: VSPA kernels can be written in C or optimized assembly, the underlying compiler infrastructure is open source. Together with publicly available example kernels and a documented instruction-set architecture, this enables transparent research workflows, controlled experimentation with custom PHY functions, and reproducibility on deployment-grade silicon [23]. The LimeSDR Micro VSPA firmware builds on the NXP la931x_iqplayer open-source release; the VSPA Common repository includes additional kernels—FFT/iFFT and beyond—providing a foundation for community-driven and proprietary PHY acceleration [23]. The ARM subsystem orchestrates device control, register access, PCIe configuration, and DSP task management, while the shared memory map provides low-latency exchange between ARM, DSP, and Direct Memory Access (DMA) engines without host intervention. The SoC exposes a PCIe Gen2 ×1 host interface with a dedicated DMA engine designed for continuous, low-latency complex-sample transfer.

The LA9310 integrates four 153 MS/s differential ADCs and two 153 MS/s DACs for I/Q baseband processing, plus a dedicated single-ended ADC for transmit path monitoring and on-chip calibration.

In the present 6G4All platform, the full NR PHY executes on the host processor, with the LA9310 providing PCIe-based I/Q streaming. The VSPA DSP subsystem remains available for incremental PHY offload—beginning with FFT/iFFT and channel estimation - as outlined in Section VII, enabling a progressively more self-contained baseband pipeline.

The single-digit-watt power envelope and open VSPA firmware make the LA9310 directly applicable to embedded and RedCap-class 5G/6G research beyond the laboratory. [21]

C. Lime Microsystems FPRF Transceiver and Lime Suite NG Driver

LMS7002M is Lime Microsystems' second-generation field-programmable RF (FPRF) transceiver. The RFIC integrates 12-bit ADCs and DACs, signal processing, LNAs, filters, and mixers to provide two transmit and receive paths, enabling single-chip 2×2 MIMO operation.

In the case of LimeSDR Micro, baseband ADCs and DACs are provided by NXP LA9310 and the interface with LMS7002M is via analog I/Q. LMS7002M is configured via Serial Peripheral Interface and LA9310 operates as the bus controller. The clock for LMS7002M ADCs and DACs is supplied by an integrated clock phase locked loop (PLL), which can also be used to drive external digital circuits up to 160 MHz. This feature is used with LimeSDR Micro to provide a configurable clock for LA9310. The two devices are thus architecturally complementary, minimizing external component count. Table III summarizes the key RF specifications of the LMS7002M in analog I/Q mode as used on the LimeSDR Micro. Additional digital features are available when using LMS7002M internal ADCs and DACs, such as the transceiver signal processor — this provides fixed-function DSP such as digital filtering and numerically controlled oscillator for frequency hopping — and integrated micro controller unit (MCU)-based calibration. With LimeSDR Micro, signal processing is instead provided by the LA9310 VSPA subsystem (Section III-B), which currently implements decimation/interpolation and calibration tasks such as I/Q correction.

Lime Suite NG is Lime Microsystems' next-generation driver stack, designed to support heterogeneous SDR designs integrating external ADCs, DACs, and baseband processors. [19]

Driver stack support for LimeSDR Micro includes a PCIe kernel module which is based on the NXP's `la9310shiva` driver, with numerous updates, such as support for use with a wider variety of host platforms. Lime Suite NG is responsible for initial programming — and when required reprogramming — of the LA9310's ARM M4 and VSPA cores, along

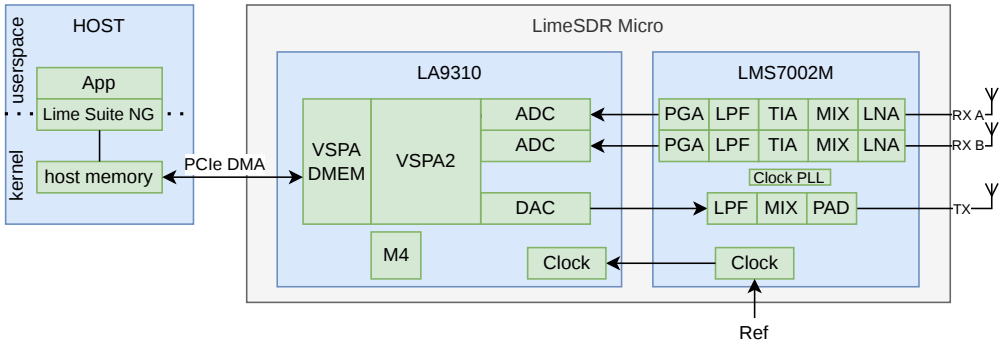

Fig. 1. 6G4All platform architecture: the LimeSDR Micro module (LA9310 + LMS7002M) with interchangeable host platforms.

TABLE III
LMS7002M KEY RF SPECIFICATIONS (ANALOG I/Q MODE).

Parameter	Value
Frequency range	30 MHz to 3800 MHz
Instantaneous bandwidth	Up to 100 MHz
Analog filter range	0.7 MHz to 108 MHz
MIMO configuration	2×2
EVM	$< 2\%$
Noise figure	< 3 dB
Tx power (OFDM, −50 dBc ACPR)	3 dBm max
Phase noise	0.5° (ref. source dep.)

with configuring the SDR and as part of which performing automatic calibration.

Lime Suite NG exposes native APIs, a compatibility wrapper for classic Lime Suite, and plug-ins for SoapySDR and GNU Radio, integrating the LimeSDR Micro into the broad existing SDR ecosystem.

D. Key Advantages

Modular and affordable. The PCIe form factor allows the identical SDR module to operate in hosts from compact embedded systems to high-performance servers without hardware modification. At a target retail price of under 300 $ —below the entry price of the USRP B210 (1400 $ [12])— the platform provides comparable RF capabilities at lower cost and on production-grade silicon, with identical software across all hosts.

Market-ready hardware and transfer readiness. The NXP LA9310 is a production-grade cellular baseband SoC manufactured at commercial scale [21], [24], [25]; research is therefore conducted on deployment-grade silicon, eliminating the re-engineering step that FPGA-based platforms impose before any commercial transition.

Standards-compatible. The `limesuiteng_lib` plugin implements the `openair0_device` interface used by all OAI-supported radios, inheriting OAI's 3GPP conformance without modification to upper-layer software. The LMS7002M covers 30 MHz to 3800 MHz, encompassing all 3GPP FR1 bands; the LA9310's 153MS/s ADC/DAC supports wide bandwidths, with the primary target—3GPP RedCap (20 MHz max FR1)—fully covered by the demonstrated 10 MHz, and wider operation subject to LimeSuiteNG RF calibration tables and host compute headroom.

Scalable and embedded-deployable. The low per-unit cost enables testbed scales that are economically infeasible with high-end SDR platforms: a 50-node deployment costs approximately 15 000 $ versus 70 000 $+ with USRP B210 nodes [12]. The M.2/PCIe form factor further enables embedded edge deployments—drones, vehicles, robots—physically incompatible with rack-mounted FPGA hardware.

OpenSource Hardware and Software. The complete platform stack is open-source: OAI provides the 3GPP-conformant protocol stack, Lime Suite NG the driver and RF abstraction layer, and the LimeSDR Micro PCB design files and VSPA DSP firmware are published under permissive licensing with open compiler toolchain and community kernel repository [23].

IV. INTEGRATION WITH OPENAIRINTERFACE

A. OpenAirInterface as a Reference Stack

OAI is an open-source initiative that implements 3GPP and O-RAN compliant networks for experimental and prototyping work in cellular networks [6]. It encompasses a set of software projects providing RAN, CN, and UE components. OAI enables the deployment of a complete 5G NR stack, including a CN following 3GPP's service-based architecture, a gNB with functional splits across CU, DU, and RU components, as well as support for 3GPP-compliant UEs and OAI's own UE. The project is supported by a large and active, international community, and is released under a 3GPP-compatible open-source license. These characteristics have established OAI as a de-facto standard for open cellular software in research and industry, stewarded by the non-profit OAI Software Alliance. Beyond this core functionality, OAI further integrates with the broader ecosystem, including compatibility with O-RAN architectures including near-real-time RAN intelligent control via OAI's own FlexRIC. A continuous integration and continuous delivery pipeline ensures the quality of stack and a seamless integration of new features. Finally, OAI abstracts underlying radio hardware through a flexible radio device driver interface that allows a wide range of SDRs and O-RAN-compatible radio in diverse deployments.

Collectively, these features make OAI a key enabler for open and flexible 6G research and a natural software partner for the 6G4All SDR platform.

B. Integration Architecture

The OAI 5G NR stack decouples radio hardware through a radio device driver interface: at runtime, gNB and UE dynamically load a radio-specific shared object implementing RF control and I/Q streaming against the `openair0_device` hardware abstraction layer. This mechanism is used by the widely-deployed USRP backend, where `usrp_lib` wraps the UHD host driver [26] in exactly the same plugin role. The 6G4All integration provides `limesuiteng_lib`—a new `openair0_device`-compliant plugin that wraps the Lime Suite NG driver API [19] to expose the LimeSDR Micro's transceiver and path to the OAI stack. Neither gNB nor UE require any modification; all integration is contained within the plugin boundary and thus transparent to the stack, leaving the upper protocol layers unchanged. The current integration runs the complete NR PHY on the host CPU; incremental offload of PHY functions to the LA9310 VSPA DSP cores is described as future work in Section VII.

V. The 6G4All Initiative and Platform Context

The 6G4All initiative is an international effort to accelerate 5G and 6G adoption through standards-compatible, open E2E solutions built exclusively on hardware deployable in commercial products [4]. It covers the complete mobile chain from terminal through RAN to core, drawing on a partner ecosystem spanning chipset design (NXP Semiconductors, NL), transceiver and driver development (Lime Microsystems, UK), open-source protocol stack (OpenAirInterface Software Alliance, FR), and system integration and research (DFKI, DE). The experimental system in Section VI uses the complete OAI E2E stack: `nr-softmodem` gNB, `nr-uesoftmodem` UE, and the OAI CN5G core [27]. The initiative roadmap targets core-agnostic operation: the planned integration of Fraunhofer FOKUS' Open5GCore [28] as an alternative core exemplifies this direction, ensuring the RAN platform is not tied to a single core implementation.

Platform guides and resources are published at [4], [19], [29], [30].

VI. Experimental Validation

Three configurations validate complementary operating points, all in SA mode with CN5G co-located on the gNB host: S1 uses $\mu = 0$ (15 kHz SCS) at 20 MHz over an over-the-air RF path; S2 and S3 use $\mu = 1$ (30 kHz SCS) at 10 MHz over a conducted RF path. E2E IP throughput is measured via `iperf3` and round-trip latency via ICMP ping (100 packets). Table IV maps outcomes to the platform claims of Section III-D; Tables V and VI define setup aliases and KPIs.

Three hardware configurations are identified by the aliases in Table V: S1 provides a high-headroom x86 baseline at 20 MHz with a COTS UE over the air; S2 applies FDD Band 5 at 10 MHz on an ARMv8-A host at the lower bound of OAI CPU frequency guidance (2 GHz); S3 evaluates TDD in a symmetric all-LimeSDR Micro configuration on ARMv8-A.

TABLE IV
Claim validation summary.

Claim	Evidence	Status
E2E IP on commercial SoC	B5 ping+iperf3	✓
Multi-band FR1	B5 + B41 (ping)	✓
FDD and TDD	Both demonstrated	✓
Stds. interoperability	Lime gNB + Quectel RM520N	✓
Dual role: gNB and UE	gNB stable; UE partial	*Partial*
ISA portability	Lime gNB on x86	✓
Edge host (i.MX95)	SSB+RA Msg. 3; IP pend.	*Partial*

TABLE V
Experimental setup configurations.

Code	Role / Band / Duplex	Hosts
S1	Lime gNB + Quectel RM520N / B5 / FDD (20 MHz, OTA)	Ryzen 9 7950X (x86)
S2	Lime gNB + B210 UE / B5 / FDD	LX2160A (ARMv8-A)
S3	Lime gNB + Lime UE/ B41 / TDD	LX2160A + LX2160A

Table VI reports the primary quantitative results. Ping latency is given as average with mean deviation (mdev) over 100 ICMP packets. Downlink throughput is measured with `iperf3` UDP where applicable; S3 was evaluated for connectivity and latency only.

Observations and Takeaways. S1 demonstrates robust SA attach and sustained IP connectivity on Band 5 at 20 MHz with a COTS UE (Quectel RM520N) over the air, achieving 14.3 ms ping (mdev 2.9 ms) and 88.1 Mbit/s DL over 100 s. S2 attains Band 5 operation on ARMv8-A at 10 MHz; the reduced DL ($\sim$1.0 Mbit/s) and UL instability are consistent with the OAI CPU frequency lower bound [20]. S3 establishes Band 41 TDD connectivity in a symmetric Lime–Lime configuration; the high ping mdev (242.5 ms) and session drops after 30–120 s are observed under the same ARMv8-A host configuration, with TDD's strict slot-switching timing requirements a plausible contributing factor. The i.MX95 (ARMv8.2-A, 6$\times$Cortex-A55 at 1.8 GHz, below the OAI minimum) achieves SSB synchronization and random access procedure through Message 3; full IP connectivity was not attained, consistent with the platform's compute floor being exceeded at this clock frequency. Three driver-layer features that are not yet fully implemented—RF gain-path calibration and automatic gain control (AGC) in Lime Suite NG, PHY-clock-aligned sample timestamps for timing advance and TDD slot switching, and PHY offload to the LA9310 VSPA cores—are candidate explanations for the observed throughput ceiling and session instability, though their individual contributions cannot be isolated from the current results.

VII. Roadmap and Conclusion

Near-term development targets the two driver-layer items identified as candidate limitations in Section VI: completing RF gain-path calibration and AGC in Lime Suite NG, and

TABLE VI
KPIs BY SETUP.

Code	Avg. Ping (mdev) [ms]	DL [Mbit/s]	Stability
S1	14.3 (2.9)	88.1	stable
S2	26.3 (2.6)	∼1.0	unstable
S3	108.0 (242.5)	—	unstable

implementing PHY-clock-aligned sample timestamps—both requiring only software work, as the LA9310's integrated PHY timer already provides the hardware foundation for sample-accurate timing. Band 78 (3.5 GHz) is deferred pending completion of the corresponding LMS7002M wideband calibration tables in Lime Suite NG. Channel bandwidth is secondary to the target deployment class: the 3GPP RedCap profile maximum bandwidth of 20 MHz FR1 [31] is directly confirmed by the S1 measurement; wider bandwidths are architecturally supported but outside the 3GPP RedCap scope of this work.

The most impactful medium-term development is incremental PHY offload from the host CPU to the LA9310 VSPA DSP cores: currently all NR PHY processing—FFT/iFFT, LDPC, channel estimation—executes on the host, with the LA9310 handling I/Q streaming only. Offloading FFT/iFFT and LDPC decoding first—the dominant compute consumers—will reduce the host CPU requirement sufficiently to enable full IP connectivity on the i.MX95 and comparable embedded hosts, unlocking the edge deployments that motivate the M.2/PCIe form factor: drones, autonomous vehicles, and mobile robots. Subsequent offload of channel estimation and precoding targets fully self-contained embedded RAN nodes.

In summary, this paper has presented the 6G4All SDR platform—a fully open-source, compact M.2/PCIe module combining the NXP LA9310 commercial baseband SoC with the Lime Microsystems LMS7002M RF transceiver, integrated into the 3GPP-conformant OAI 5G NR stack without modification to upper-layer software. E2E IP connectivity has been demonstrated across two FR1 bands and both FDD and TDD duplexing modes, providing the first experimental validation of standards-compatible 5G NR operation on a production-grade cellular baseband SoC with a commercial UE: a platform that closes the transfer gap between open research and commercial deployment.

ACKNOWLEDGMENT

This work has been supported by the Federal Ministry of Research, Technology and Space of the Federal Republic of Germany (Grant agreement number 16KIS2402K, Open6GHub+). The authors alone are responsible for the content of the paper.

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